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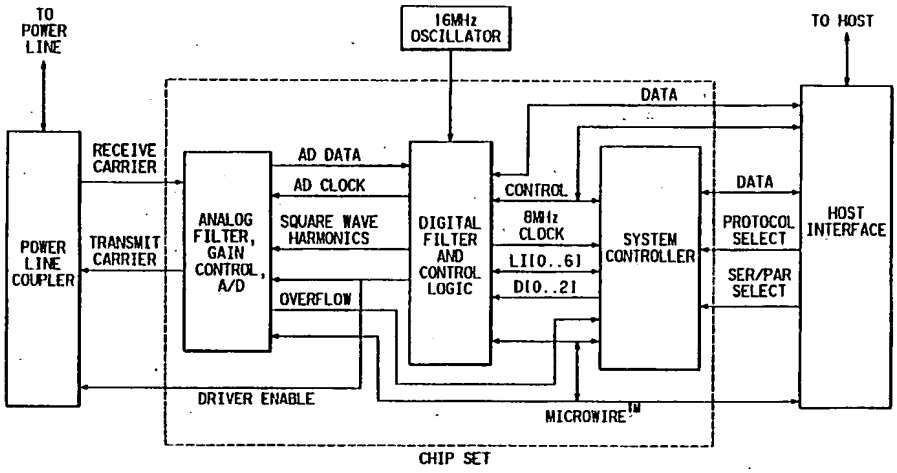

(57) Abstract

A system utilizing adaptive frequency-hopped spread spectrum modulation to communicate over noisy communications channels is described. Individual packets of data are transmitted with FSK modulation using two frequencies chosen from a larger set. An error coding system is used in which data on the quality of reception at each network transceiver is used to alter the gain of the receiver, the bit rate of the transmission, and the specific frequencies employed by the network for the purpose of optimizing communicatioin error rate. A Master transceiver, controlling network management, transmits channel control information to other transceivers on the network, enabling system synchronization, acquisition of an existing network by new subscribers. Each transceiver comprises a frequency controlled carrier generator, a pair of digital detectors each having a frequency controlled bandpass filter microprocessors for control and broad band coupling networks for coupling the transceiver to a communications channel.

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FREQUENCY HOPPING TIME-DIVERSITY COMMUNICATIONS SYSTEMS AND TRANSCEIVERS FOR LOCAL AREA NETWORKS

RELATED APPLICATIONS

This application is a Continuation-in-Part of United States Application No. 07/333,336, filed April 5, 1989 which application was a Continuation-in-Part of United States Application No. 07/309,272, filed February 10, 1989, which application was a Continuation-in-Part of United States Application No. 07/115,245, filed October 30, 1987, which application was a Continuation-in-Part of Application No. 06/846,924 of April 1, 1986, now abandoned, which application was a Divisional Application of United States Application No. 06/586,863 of March 6, 1984, now United States Patent No. 4,597,082, issued June 24, 1986; the above applications and patent are incorporated herein by reference.

TECHNICAL FIELD

This invention relates to spread spectrum-time diversity communications systems and transceivers for multidrop local area networks. Such transceivers may be used for communication over power lines, twisted pairs, over wires lain along the path of guided vehicles, or the like. The invention further relates to the transmission of digital data in industrial environments over transmission channels having noise characteristics influenced by the industrial environment.

BACKGROUND ART

In the above-identified United States Patent No. 4,597,082, there is disclosed a transceiver for multidrop local area networks for transmission over AC transmission lines, private wire, or other less noisy transmission channels that provides error free transmissions at very high data rates in noisy industrial environments at low cost.

In the above-identified application, Serial No. 07/115,245, there is disclosed a transceiver system for communication over wire laid along the path of guided vehicles, where in the transmission channel, is the typical floor loop used to guide such vehicles. In Serial No. 07/309,272, filed February 10, 1989, entitled Transmission Line Termination of Guide-Communications Wire For Guided Vehicles, the problem of null positions in such floor loops, at which the strength of signals sent from the host modem, is so low or non-existent that communications is impossible with the guided vehicle and one solution to that problem are discussed.

The present invention is directed to eliminating such multipath problems in wire guided vehicle applications and to combating periodic impulse and slowly time varying continuous wave noise typical of wire guided vehicles, power line carrier transmission systems and other transmission channels in an industrial environment.

While, according to the prior art, spread spectrum (frequency hopping) systems and time diversity techniques have been utilized to overcome transmission problems caused by random noise, which may be natural or caused by jamming, such techniques have not been utilized in low cost systems, which are oriented towards adaptive avoidance of inadvertent man-made noise, such as in the industrial environment. Such noise is time varying, but not truly random.

DISCLOSURE OF THE INVENTION

The transceivers of the present invention use adaptive frequency hopping to eliminate the effects of multipath and standing waves and to avoid time-varying continuous wave noise. The transceivers also utilize error correction coding to combat impulse noise.

In one embodiment of the invention, 8 frequencies are utilized in a frequency band from 20 kHz to 90 kHz. These frequencies are chosen, such that the side bands of the frequencies, when modulated as described herein, do not overlap. Manchester encoding of the digital bit stream is employed, wherein a transition between carrier frequencies occurs once per bit.

Each information byte of consists of eight information bits plus one parity bit providing limited error detection. The entire packet is also protected by a 27 bit error detection code.

The transceiver according to the invention is provided with a protocol program and an I/O program, which may operate on separate microprocessors or through time sharing on a single processor. In the transmit mode, the I/O program transmits a frequency code to a digital counter which changes its counting modulus so as to produce the correct frequency for transmission, which is then gated and wave-shaped under control of data supplied by the physical I/O program.

During reception, the I/O program provides a frequency code to a pair of frequency controlled filters which pass the appropriate frequency to the digital filters, which use the appropriate clock signals derived from the clock logic to receive the transmitted frequencies.

According to the invention, detection of an uncorrectable error after the spread spectrum transmission of a data block will cause the receiver to transmit an error message to the sending transceiver, which will retransmit the data block. When a block is received with such an uncorrectable error in one or more bytes, the correct bytes are stored in a buffer, so that when the repeated transmission is received, it is only necessary that those

bytes having errors the first time be received correctly the second time. In such a case, the final 27 bit error detection code is used to verify that the combination of multiple partially received transmissions has occurred correctly. Thus, it is possible for the receiver to correctly receive a block, even though that block is never received without errors.
Means are provided for initializing the system so that all transceivers are operating on the same pair of frequencies at the same time.

Means are provided for measuring the raw bit error rate; Receiver gain is adjusted based upon the measured error rate performance.

In the event that gain adjustment does not produce an acceptable error rate, the data rate in use is reduced. If, after reduction to the lowest implemented data rate, the error rate is still unsatisfactory, a different transmission frequency will be employed. Similarly, good error performance will result in an increase in data rate. Information on bit rate and frequency is conveyed to all subscribers on the network through the channel control field in the message packet.

The data packets transmitted contain a master address field, which may be used to provide for multiple, frequency-division multiplexed networks functioning concurrently on the same physical transmission medium. Means is provided in the frequency shifting algorithm to treat transmissions with a different master address in the same way as noise, resulting in automatic switching to a differ-

ent frequency.

The hardware to implement this invention consists of five elements, shown in simplified block diagram form in Figure 1. A schematic of the actual circuitry is shown in Figure 2 through 5.

The major elements of the design are:

The control microprocessor, which implements the channel control algorithms described above, controls external interfaces, and implements physical, link, and network layer protocols.

The digital subsystem, which includes hardware for the external interfaces, timing and clock generation logic, transmit signal generation logic, and the digital portion of the receiver, including digital filtering and data recovery.

The analog subsystem, including a broad-band, high-gain front end with digital control of the gain in multiple steps, an Analog to digital converter for the signal, and analog circuitry to feed and control the transmit power amplifier.

External components, including host interface circuitry, coupling to the AC power line, impulse protection circuitry, and the transmit power amplifier.

OBJECTS OF THE INVENTION

It is therefore an object of the invention to provide improved communications in an environment of slowly time varying continuous wave noise and constant frequency impulse noise.

Another object of the invention, is to provide such communications utilizing spread spectrum and time diversity techniques.

A further object of the invention, is to provide for such communications in industrial environments over power lines, dedicated pairs, automated guided vehicle floor loops, and similar noisy transmission channels.

Another object of the invention, is to increase the data rates in such communications.

A still further object of the invention, is to reduce error rates in such communications.

Another object of the invention is to provide a technique for data communication and ranging which can be implemented in inexpensive integrated circuit form and which will exhibit very high resistance to impulsive and continuous-wave noise interference.

A further object of the invention is to provide a reliable means of communication over AC power lines, which exhibit such noise characteristics.

Other objects of the invention, will in part be obvious and will in part appear hereinafter.

The invention accordingly comprises the features of construction, several elements, the arrangements of parts, and the choice of functions and signals, which will be exemplified in the construction of the systems hereinafter set forth. The scope of the invention is indicated in the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

For a fuller understanding of the nature and objects of the invention, reference should be had to the following detailed description, taken in connection with the accompanying drawings, in which:

FIGURE 1 is a block diagram of a spread spectrum time-diversity communication system transceivers according to the invention;

FIGURE 2 is a schematic circuit diagram of the chip set of Figure 1 connected for parallel communication with the host of Figure 1;

FIGURE 3 is a schematic circuit diagram of the chip set of Figure 1 connected for serial communication with the host of Figure 1;

FIGURE 4 is a schematic circuit diagram of the power line coupler of Figure 1;

FIGURE 5 is a schematic circuit diagram of configuring switches and light emitting diode indicators connected to the chip set of Figure 1;

FIGURE 6 is a detailed block diagram of the digital chip and digital subsystem of Figure 1;

FIGURE 7 is a detailed block diagram of the analog chip of Figure 1;

FIGURE 8A is a conceptual block diagram of the gain setting logic of the invention;

FIGURE 8B is a conceptual block diagram of the bit rate and frequency choosing logic of the invention;

FIGURE 9 is a flow chart of the gain control logic of the system shown in Figure 1;

FIGURE 10 is a graph of error rate versus gain illustrating operation of the gain control logic;

FIGURE 11 is flow chart of the bit rate logic of the system of Figure 1;

FIGURE 12 is a flow chart of the frequency hopping logic of the system of Figure 1;

FIGURE 13 is a flow chart of the slave network acquisition logic of the system of Figure 1;

FIGURE 14 is a flow chart of the master network acquisition logic of the system of Figure 1;

FIGURE 15 is a flow chart of the packet overlay logic of the system of Figure 1; and

FIGURE 16 is a diagram of the packet format used in the system of Figure 1.

The same reference characters refer to the same elements throughout the several views of the drawings.

BEST MODE FOR CARRYING OUT THE INVENTION

This section describes the specific design of the system in detail.

The hardware is first discussed in detail with reference to a chip-level schematic, and then in more detail, referring to the internals of the chips.

The operation of the software algorithms controlling operation of the system are then described, first in general terms and then in detail with reference to specific routines.

HARDWARE SYSTEM DESCRIPTION

This section describes major hardware elements of the system. Figures 2 through 5 comprise a schematic of the system, and partition it into the functional blocks shown in Figure 1.

CONTROL MICROPROCESSOR

A National COP-series microprocessor, U6 of Figure 2, is employed. It interfaces primarily to the digital chip, U7 of figure 2, but in addition there are several pins connecting to the host interface.

Host interface pins are:SER/PAR, NET/TRANS, which are strapped by

the user to indicate unit configuration; RXRDY, TXRDY, which relate to an 8-bit parallel interface to the user; RTS/COMMAND, CTS/STATUS, RCD, and TXD, which comprise a serial interface to the user with bidirectional flow control.

Interfaces to the digital chip include a RESET; SO, SI, and SK are used in the standard Microwire serial interface configuration described by National Semiconductor; RAW DATA, received data prior to Manchester decoding, LRCD and LTXD clocks for receive and transmit, PTT to control direction (receive or transmit); and WDT, a watch dog timer which shuts the system down in the event of certain failures.
Other information related to bit rate and frequencies is transferred to the digital chip via the microwire interface.

DIGITAL SUBSSYSTEM

The digital chip is shown in block diagram form in figure 6.

The system is driven by an external 16 MHz crystal. The crystal clock feeds a pair of binary rate multipliers, whose output frequencies are controlled by data written into their counters by the control microprocessor. The output of the binary rate multipliers feeds a timer chain which generates two designated carrier frequencies, as well as their third, fifth, and seventh harmonics. These harmonics are added together with the fundamental carrier, appropriately weighted, in the analog chip to produce a nearly sinusoidal carrier. In addition, several clocks are derived for data reception and decoding: for each of the two designated

frequencies, both in-phase and quadrature clocks are developed; and clocks for the low pass filters and for the bandpass filters are generated, whose frequency is determined by the bit rate commanded by the microprocessor.

Transmission is controlled by the microprocessor, through PTT (push-to-talk) pin which enables output, and through the data pin which controls the output of one or zero. Data provided by the microprocessor is manchester-encoded by the microcontroller, which outputs the appropriate carrier sequence together with its harmonics.

The received signal enters the digital chip as a 3-bit digitized signal, plus overflow from the analog chip's A/D converter. This data is run in parallel through four mixers, for in-phase and quadrature components of each of the two designated frequencies. These are implemented by exclusive-OR of the input with the clocks.

The I and Q components are then run in parallel through four low-pass filters, to generate magnitude signals for each. The results are fed to a system of comparators, which compares the sum of I and Q energy on each of the two frequencies, and outputs a signal corresponding to the frequency with higher energy. This is a representation of manchester-encoded data; it is decoded and output as data to the microprocessor (manchester-encoded data is also available to the microprocessor, but is not currently used).

Bit synchronization is obtained through a bandpass filter feed-

back loop, which uses an initial synchronization pattern at the beginning of each packet to lock onto the f0-f1 transitions in the received signal, and synchronizes the integrate-and dump function in the comparator and the Manchester decoding accordingly.

ANALOG SUBSYSTEM

Figure 7 is a block diagram of the analog chip. It shows the receive filter broadband operational amplifiers, which are connected through external resistors and capacitors as shown in Figure 3. The broadband filtering is accomplished through series low pass and high pass elements. Inputs C0 through C2 switch difference values of feedback resistors into the gain path, permitting gain to be set in 6 db steps from 3 to 60 db. This signal is then fed to the A/D converter, an conventional flash converter design clocked at 1 Mhz. (Its digital portion is in the digital chip.

On the transmit side, FSQWV, 3F, 5F and 7F clocks are combined in the wave-shaper, which adds them together with appropriate relative gain to approximate a sine wave of frequency of FSQWV. This is passed through an additional filter stage, and then to the driver which interfaces to the external power amplifier/driver stage.

TRANSMIT CARRIER POWER AMPLIFIER

This section amplifies the output of the transmit carrier genera-

tion logic and applies it to the AC line coupling network. It consists primarily of Q1 through Q4 shown on Figure 4, and is straightforward.

AC LINE COUPLING NETWORK

This passive network provides coupling to the AC line. It is designed to provide relatively little voltage drop and phase distortion when presented with the power line's impedance at 20 to 90 KHz. It is shown in Figure 5.

For input signals from the AC line, the coupler is designed to attenuate 60 Hz by at least 100 db, provide reasonably flat frequency response across the operating range of 9 - 90 KHz, present a high impedance to the line in the operating frequency range, and avoid ringing in response to high energy impulse noise. Protection is provided by MOV1, D1,D2, D3.

SUPPORTING HARDWARE

The board version of the system includes a power supply, and various LEDs and dip switches intended to facilitate installation. These are detailed in Figures 4.

PHYSICAL LAYER OPERATION: NETWORK CONTROL SYSTEM

This section describes the processes involved in control of physical layer communications.

The processes discussed are:

Frequency hopping control
Gain optimization
Bit rate optimization

Frequency optimization
Synchronization and network acquisition
Error coding and time diversity

Together, these processes comprise a feedback control system which causes communications to operate in that portion of the available spectrum which will permit the greatest data rate to be used with acceptable error rate.

The general structure of the feedbackloops is shown conceptually in Figure 8.

FREQUENCY HOPPING CONTROL (BIT LEVEL)

This section describes the spectrum allocation, the coding of information bits, and the processing required for system manage-

ment at the bit level.

Spectrum Allocation

Consistent with the CENELEC proposed standard, the system will operate within the band of 9 - 90 KHz.

Another consideration in the choice of frequencies is that they be so spaced that the principal harmonics of one do not lie close to another, so that distortion in the transmitted waveform of one carrier will not cause interference with another frequency channel. At the same time, it is necessary that these be generated from a common high-speed clock with different divisors, in order to maintain reasonable simplicity in the timing logic.

Definition of Tones

Each bit is encoded as a combination of two frequencies, together comprising a manchester-encoded bit of information.
It is desirable to set up the channels to be contiguous but nonoverlapping, to take full advantage of the available spectrum without making two adjacent channels vulnerable to the same single-frequency noise source. This leads to the following frequency allocation:

tune	f0 (Hz)	f1 (Hz)
0	76200	50800
1	57142	38095
2	42857	28571
3	32142	21428

Tune Control

The microprocessor will load a code for each of the two frequencies of the current tune.

AUTOMATIC GAIN CONTROL

The gain associated with each frequency is adjustable, based on bit error rate as measures over a small number of packets. This section describes the process.

In the master, this loop is fast compared to the bit rate and frequency change loop; that is, changes to gain are made more readily than changes to bit rate and frequency, to avoid thrashing between the two dimensions of the system.

Upon reset, prior to network acquisition, the gain is set at its middle value. It is then adjusted based on the occurrence of bytes received in error, as determined by the parity bit. A

change is made to the gain after each four packets received. Since a gain setting either too high or too low will produce inferior performance, a two-step peak-finding algorithm is used:

1. measure error rate at current gain value
2. change gain and measure error rate
3. if error rate is better, change gain again in same direction; if error rate is worse, return to previous setting (peak found)
4. when a peak is found, stay at same setting for 16 packets, then repeat process.

This process is described in greater detail in Figure 9, a flow chart for the gain control algorithm, and Figure 10, a chart showing the sequence of gains which would be chosen with a hypothetical but typical relationship between gain and error rate. The curve in Figure 11 indicates an optimum gain between gain = 2 and gain = 3, with worse performance at either higher or lower values of gain. This is typical of actual performance, since too high a gain will saturate the receiver with noise, while too low a gain will place the signal below the receiver's threshold. The numbers in circles on both figures indicate the sequence of events:

The system starts operating at a gain of 4, and measures the error rate for four successive received packets (1). Upon initialization, the variable "bit error rate" was set to zero, so

when the new measurement is compared to the previous bit error rate, it will be worse (2). This causes the variable "direction" to be reversed in sign, it is then +1. Thus, the gain is incremented to a value of 5, (3) and error rate is measured for another four packets (4). In our example, a worse measurement is obtained, causing direction to be again reversed to -1, (6) and gain set to 4, (7). The next measurement (8) produces another improvement in error rate (9), so gain is again decremented (10) to 3. The next measurement (11) again improves gain (12), and gain is again decremented (13) to 2. Now the optimum has been passed, the next measurement (14) is worse than the preceding one, so gain is incremented instead of decremented, not to a value of 3, (16). The system, having found the peak, now stays at this value of gain for 16 packets, instead of four, and then repeats the entire process. This longer sample time after a peak is found improves the systems performance, because less time is spent at the sub-optimal gain values surrounding the peak. The length of the on-peak sample time is limited, however, by the need to make the system responsive to frequent changes in the ambient noise environment, and in received signal strength.

BIT RATE OPTIMIZATION

The slave controls its gain autonomously, but changes bit rate and frequency only in response to a command from the master, or during network acquisition, if it loses the network or has just been powered on. The following discussion thus applies only to the master.

The master starts at the highest bit rate. A figure of merit for

network performance is maintained as follows, and is updated each time a packet is received:

BRCNT(N) = BRCNT(N-1) + 1 if packet retry occurs

= BRCNT(N-1)/2 if packet received without retry

BRCNT is an 8 bit number. If BRCNT exceeds a upper threshold, then the bit rate is decreased, unless the lowest bit rate is already in use. In this case, frequency is changed. If BRCNT drops below a lower threshold, then bit rate is increased. If bit rate is maximum, only the first threshold applies.

This is illustrated as a flow chart in Figure 11. Each time a packet is received, a change is made to the BRCNT variable. The effect of a correct packet is stronger than the effect of an incorrect packet; it reduces the count by a factor of two (see (2) on Figure 11). The new value of the BRCNT variable is compared with a threshold, and bit rate increased, unless already maximum, when the threshold is reached (3).

Similarly, a series of bad packets will increase BRCNT (4), and produce a decrease in bit rate when an upper threshold is reached (5). If the logic calls for a lower than the lowest bit rate, then the frequency channel change algorithm is invoked (6).

FREQUENCY OPTIMIZATION (TUNE SELECTION)

The master starts the network at the highest frequency channel

not occupied by another master address. It will drop to another frequency channel is the system is currently operating on the lowest bit rate, and a figure of merit, FHCNT, exceeds a threshold. FHCNT is calculated similarly to BRCNT, as a function of packet retries. The master will rotate through available frequency channels; collision with existing networks with other master addresses will be treated in the same way as unacceptable FHCNT, resulting in shift to another frequency channel. The logic is shown in Figure 12.

BIT RATE AND TUNE CHANGE COMMUNICATION TO SLAVES

The current bit rate and frequency are designated in each packet. When a change is requested by the master, it transmits four packets with the new code on the old bit rate and frequency, and then changes to the new set. Those slaves hearing the packets change immediately; those that do not lose the network, and enter the network acquisition routine.

SYNCHRONIZATION AND NETWORK ACQUISITION BY SLAVES

This section describes the process through which a network is initialized, and through which additional subscribers join the network.

Slave Initialization

Upon initialization, a slave must search for and find the tune and bit rate currently in use. It proceeds as described below, and illustrated in Figure 13.

All tunes are searched, starting with the highest. Within each tune search, bit rate is searched, starting with the highest. Within each bit rate, gain is searched highest to lowest. If a valid (error code checks correct) sequence is obtained during this process, then the slave knows the tune and switches to it, entering run mode. If not, the slave proceeds to search the tunes bit rates and gains, remaining on each combination for four packet times. This process is repeated until a valid packet is received.

Master Initialization

The master starts by performing the slave initialization sequence to see if a network with the same network address already exists. If so, it is internally disabled. This is intended to prevent seizure of a network by a master in malevolent hands.

If the master cannot find a slave with its own network address, it will proceed to the next frequency channel, and repeat the process. This is shown in Figure 14.

Network Runtime Operation

In order to keep the system gain and tune selection optimal, the network will always be active. In network mode, the master runs internal test (software loopback) whenever there is no host traffic required.

Software loopback or test mode will operate as follows: For the first cycle, the master will attempt to access all 255 slave addressees. Subsequently it will scan only up to the highest address which responded. Every TBD cycles, it will search the full set. (It is required that the user pack addresses contiguously upward from 1 for efficient operation). Each time it accesses a slave, it will send a packet of test data which the slave will echo. The master will process to the next slave address upon correct receipt of the echo.

Once a network is established with one or more slaves, the tune control will be performed as described above.

ERROR CODING AND TIME DIVERSITY

In addition to frequency-dependent noise which will be combated by the adaptive frequency hopping described above, power lines are characterized by impulsive noise, which by definition occupies all frequency bands for relatively short periods, often less than one bit time. This noise, tends to be 100 or 120 Hz synchronous, due to its origin.

In network mode and in the software loopback function of transparent mode, two techniques are employed to reduce sensitivity to impulse noise: error detection coding, and saving those bytes of a block which were not corrupted, so that on a subsequent retry a

complete message will exist at the receiver unless the same portion is hit on successive tries. The timing of successive tries is arbitrary due to variable block length, and it is likely that 100 or 120 hz synchronous disturbance will not hit the same message portion on successive attempts.

Error Correction

A 27 bit error code is employed, consisting of three bytes plus byte parity. They consist of a cumulative XOR of the bytes in the packet, followed by an XOR of the bytes in the packet with a one-byte left rotate after each byte is added, followed by an XOR of the bytes in the packet with a right rotate after each XOR. This allows implementation in software in real time, and provides good performance with the overlay technique. In implementations with a more powerful processor, a stronger code will be appropriate.

Overlay of Retries

If a given byte of a packet can not be corrected, the receiver will continue to collect data for the remainder of the packet, and will store those bytes subject to successful error correction in the receive buffer. However, if the first byte, which contains the packet length, is corrupted, the packet must be abandoned.)

On subsequent retries, if a byte is in error, it will not be

written to the receive buffer, but the byte already stored from the previous retry will be incorporated in the running checksum. At the end of the packet, if the checksum is found to be valid, then a complete valid packet has been assembled from two or more transmissions, and it will be processed as such. This logic is shown in detail in Figure 15.

This approach allows the system to communicate successfully even in a noise environment which precludes a packet from ever being received with only correctable errors, as long as each byte gets through once.

LINK LEVEL OPERATION

This section describes the operation of the link layer of the system, separately for transparent mode and network mode.

TRANSPARENT MODE

Transparent mode is extremely simple: Data transmitted into the master by its host is transferred to the network as a modulated bit stream, which is decoded by all slaves which can hear it and output as serial data to their hosts. Similarly, data transmitted into a slave by its host is transferred across the network and comes out all other units.

There is no addressing function, error detection or correction, or bus access control implemented in the system in this mode; these must be supplied by the user.

One restriction is imposed on the host network: all transmissions must be initiated by the master. The reason for this is to allow the system to use idle periods for network optimization. This process consists of polling each slave in succession, obtaining a loopback of data, and reports of channel quality from each slave. This information is used by the physical layer routines to control gain and tune selection.

NETWORK MODE

Network mode implements a polled, master slave system capable of both cyclic polling operation and of a point-to-point connection.

Error free logical links are provided in both cases.

Protocol Syntax

Data is transferred in packets. Each packet is comprised of four bytes plus 0 to 17 data bytes, with the quantity variable. Each byte is supplemented by a parity bit. This is illustrated in Figure 16. The fields are:

sync pattern	(4 bytes)
start of frame	(SOF, 1 byte)
control_1	(CW1, 1 byte)
control_2	(CW2, 1 byte)
slave address	(1 byte)
data	(0-17 bytes)
block error detection code	(3 bytes)

The control_1 byte is further subdivided as follows:

bits 0 - 3	data byte count (0 - 15 decimal)
bit 4	ack/nak
bit 5	sequence

bit 6	new_address
bit 7	test_mode

Packets are of variable length, and the length (in terms of data bytes) is the lower nibble of the control byte.
The ack/nak bit is used to command retransmission of a destroyed block.

The sequence bit allows the system to avoid confusing retries with new data.

The new_address bit is 1 on the first block being sent to a slave in a particular link process; it signals to the slave that this is a new link.

The slave address field is used by the slave to match messages intended for it. It ignores messages not bearing its own address, with the exception of address 0.

Address 0 is used for broadcast: All slaves accept a message with this address, but none respond to it.

The control_2 byte is organised as follows:

bits 0 - 1	tune code (master); noise level (slave)
bit 2 - 3	bit rate code
bit 4	flow control nak

bit 5	master originating
bits 6 - 7	master address

The tune code is a 2-bit code denoting the tune currently in use by the network. It is followed by a another 2-bit code for bit rate.

The next bit is used by the slave to indicate that although the link is good, the slave's host is not accepting data as fast as it is being delivered, due to flow control or a difference in data rates, and that the master should therefore send no new data, although it may keep the link active.

The next bit indicates origin of the message: 1 for master, and zero for slave.

The top 2 bits of this byte specify one of 8 master (or network) addresses. These are used to allow concurrent operation of multiple, independent networks on the same physical channel without confusion, either for store-and-forward purposes or to allow increased use of the bandwidth.

In installations where there is only one network, it is also possible to use it as a key to enable content-oriented addressing.

The error code is appended at the end of the packet, and is used to verify validity of the whole packet. Different words of the packet may have been delivered on different retires of the packet in a noisy environment.

PROTOCOL SEMANTICS

The protocol implements the various link commands described below. These allow creation of three types of links:

network test

polling cycle

Continuous link

Network test can be viewed as a special case of a polling cycle, in which data is not transferred to the host device.

Polling is in turn a special case of the continuous link, in which the link is discontinued automatically after receipt of one valid packet from the slave, and the next slave in the specified range is then connected. It shares the same routines for circuit establishment and error control. These routines are essentially the same as those described in Patent 4,597,082.

HOST COMMAND SYNTAX

Additional detail follows on the structure of commands which may

be issued to the master by the master's host. The master distinguished the commands from data by the status of the control/data line.

In addition to the command responses noted, the system will assert its ERROR pin (or BREAK if in serial mode) if an illegal command or syntax is received.

The slave does not accept or act on commands except for STATUS and EXTERNAL FH. If its control/data line is in control state, it treats data received as a destination address to be included in subsequent packets. If its internal buffer (15 bytes) is filled, subsequent data will be ignored, and additional writes to the chip will produce an error.

Network Test

This mode sends a packet to each slave within the specified range; the slave performs a software loopback to the master; the master checks for errors and reports error rate. The same block-ahead acknowledgment protocol will be used as in the case of polling and transparent link communications. The primary purpose of this mode is to provide current data a spectrum performance so the FH algorithms will remain optimized in periods of low useage. It al execute until another command received.

Command response: <status><address><data>

<status><address><data> .. <EOF marker>

Status shows success or failure to communicate with indicated address. Data from slave follows address is successful; otherwise subsequent slave's report follows.

<data> denotes data which the designated slave has received since the last time it was polled, up to one full pa execute received.

Command ranponnn: <status><address><data> .. <status><address><data> .. <EOF marker>

Status shows success or failure to communicate with indicated address. Data from slave follows address is successful; otherwise subsequent slave's report follows.

<data> denotes data which the designated slave has received since the last time it was polled, up to one full packet size

Transparent Point-to-point Link

This command establishes a point-to-point, error-free, positively acknowledged link to a single slave. once it is established, data entered in the data port of either master or slave comes out the other.

Command syntax: <op code> <address>

Command response: <address> <link status>

Link status is success or failure in establishing the link.

If a link is broken after it has been establsihed, the ERROR pin will be asserted (parallel mode) or a BREAK character will be output (serial mode).

Link remains in effect until another valid command is received.

The unit contains 15 bytes of buffering. If the input data rate is such that this buffer is filled, the TRANSMIT BUFFER AVAILABLE line will not be asserted, providing flow control.

Broadcast

This command is identical to the transparent link, except that no acknowledgment is expected or received from slaves.

The broadcast address is 00. Any unit receiving data addressed to 00 will output it to its host, if it is free if errors after error correction.

Command syntax: <op code> <address>

Command response: <address> <link status>

<Link status > is always OK.

Initialization command

Upon power-up or hardware reset, the system must receive an initialization sequence or it will do nothing. This sequence tells it whether it is a master or slave. If a slave, it also tell it its address, and an address filter (applied to the destination address field in received packets) to be used in passing network data bearing other addressed to its host. If it is a master, it is told the address range over which the system is working.

If initialized as a slave, the only commands accepted are initialization and status request.

command syntax to slave: <op code><master/slave><own address><destination address filter>

command syntax to master: <op code><master/slave><low address><destination address filter>

command response: none

Status Request

Two status requests are available: chip status and link status.

Chip status indicates the current state of the chip, and may be used by the host to obtain additional information when the ERROR pin (or serial BREAK) is asserted.

command syntax: <op code>

command response <link type><flow control status><error codes to be determined>

The link status command, valid for both master and slave, causes output of current FH tune, and relative error rate data on the frequencies of the tune, each expressed as a two-byte number.

command syntax: <op code>

command response: <own address><destination address filter> <FH tune id> <f1 error rate><f2 error rate><f3 error rate>

External FH Command

This command, allows external setting of the frequency set in use. It over-rides the internal FH algorithms, for test and debug purposes, and to allow operation of the system on a fixed-frequency basis for compatibility with possible future, fixed-frequency modes.

Command syntax: <op code><frequency to use>

if "0" is entered in the frequency field, the internal FH algorithms will be re-enabled.

command response: none

External Bit Rate Command

This command, allows external setting of the bit rate set in use. It over-rides the internal FH algorithms, for test and debug purposes, and to allow operation of the system on a fixed-frequency basis for compatibility with possible future, fixed-frequency nodes.

Command syntax: <op code><bit rate to use>

if "0" is entered in the bit rate field, the internal FH algorithms will be re-enabled.

command response: none

The IC/SS™ chip set comprising the IC/SS™ analog chip ICSS™ 1003, IC/SS™ digital chip ICSS™ 1002, and the IC/SS™ controller chip ICSS™ 1001 are manufactured by National Semiconductor Corporation of Santa Clara, California. The ICSS™ 1001 chip is a programmed National Semiconductor COP884EG microcontroller that controls the adaptive gain setting, bit rate setting, frequency hopping, host interface, and link layer protocols.

The features of the invention could also be realized in hard logic or by other computer means.

It will thus be seen that the objects set forth above, among those made apparent from the preceding description are efficiently attained and since certain changes may be made in the above systems and constructions without departing from the scope of the invention, it is intended that all matter contained in the above description or shown in the accompanying drawings shall be interpreted as illustrative and not in a limiting sense.

It is also understood that the following claims are intended to cover all of the generic and specific features of the invention herein described, and all statements of the scope of the invention which, as a matter of language, might be said to fall therebetween.

Having described my invention, what I claim as new and desire to secure by Letters Patent is:

CLAIMS

1. A communications system comprising at least one receiver employing automatic gain control for receiving binary coded parity checked information in successive packets; said receiver comprising:

A) means for determining the bit error rate occurring in received packets over a predetermined sample period; and storing said rate;

B) means for comparing said bit error rate with the bit error rate in the prior sample period; and

C) means for changing the gain of the receiver in the same direction that it was changed previously if the current bit error rate is less than the previously measured bit error rate and for changing the gain in the opposite direction if the current bit error rate ise greater than the previously measured bit error rate.

2. The system defined in claim 1 and

D) means for keeping the gain at the same setting for a predetermined number of said sample periods after changing the gain in said opposite direction.

3. The system defined in claim 2 wherein said sample period is a number of packets received.

4. The system defined in claim 1 wherein said sample period is a number of packets received.

5. A communciations system comprising a transmitter and receiver wherein binary coded information packets including error codes are transmitted from a transmitter to a receiver on at least one of a plurality of modulated frequencies and the receiver transmits to the transmitter an error signal if the receiver determines that a packet was received with an error; said transmitter comprising:

A) means for setting the transmission bit rate at one of a plurality of bit rates;

B) means for maintaining a BRCNT having upper and lower limits updated as follows -

BRCNT(N) = BRCNT(N-1) + 1 if a packet was received with an error

BRCNT(N) = BRCNT(N-1)/2 if a packet was received without an error

and for decrementing the setting of said bit error rate when the BRCNT reaches said upper limit and for incrementing the setting of said bit rate when said BRCNT reaches said lower limit; and

C) means for changing at least one frequency used in the next packet transmission when the BRCNT reaches said upper limit and the bit rate used in the error containing packet was the lowest bit rate available.

6. A communication system as defined in claim 5 wherein said receivers utilize integrate and dump bit detection.

7. A communication system comprising a plurality of slave modems each connected to a host comprising:

A) means for receiving binary coded information packets on a plurality of communication channels;

B) means for searching said channels for packets containing one of a plurality master addresses and for only transmitting to its host packets containing said master address.

8. A communication system as defined in claim 7; and,

C) means for searching said channels until packets are received containing said one master address.

9. A communication system as defined in claim 7 wherein said channels comprise frequency channels.

10. A communication system as defined in claim 1 and

D) a master modem having a specific master address and comprising

a) means for searching said channels for and, disabling itself when, a packet is received containing its master address from another master.

11. A communciations system as defined in claim 1 further comprising a transmitter and wherein binary coded information packets including error codes are transmitted from the transmitter to the receiver on at least one of a plurality of modulated frequencies and the receiver transmits to the transmitter an error signal if the receiver determines that a packet was received with an error; said transmitter comprising:

A) means for setting the transmission bit rate at one of a plurality of bit rates;

B) means for maintaining a BRCNT having upper and lower limits updated as follows -

BRCNT(N) = BRCNT(N-1) + 1 if a packet was received with an error

= BRCNT(N-1)/2 if a packet was received without an error

and for decrementing the setting of said bit error rate when the BRCNT reaches said upper limit and for incrementing the setting of said bit rate when said BRCNT reaches said lower limit; and

C) means for changing at least one frequency used in the next packet transmission when the BRCNT reaches said upper limit and the bit rate used in the error containing packet was the lowest bit rate available.

12. A communication system as defined in claim 11 comprising a plurality of slave modems each connected to a host comprising:

A) means for receiving binary coded information packets on a plurality of communication channels;

B) means for searching said channels for packets containing one of a plurality master addresses and for only transmitting to its host packets containing said master address.

13. A communication system as defined in claim 12 and

D) a master modem having a specific master address and comprising

a) means for searching said channels for and, disabling itself when, a packet is received containing its master address from another master.

14. A communication system as defined in claim 1 comprising a plurality of slave modems each connected to a host comprising:

A) means for receiving binary coded information packets on a plurality of communication channels;

B) means for searching said channels for packets containing one of a plurality master addresses and for only transmitting to its host packets containing said master address.

FIG. 1

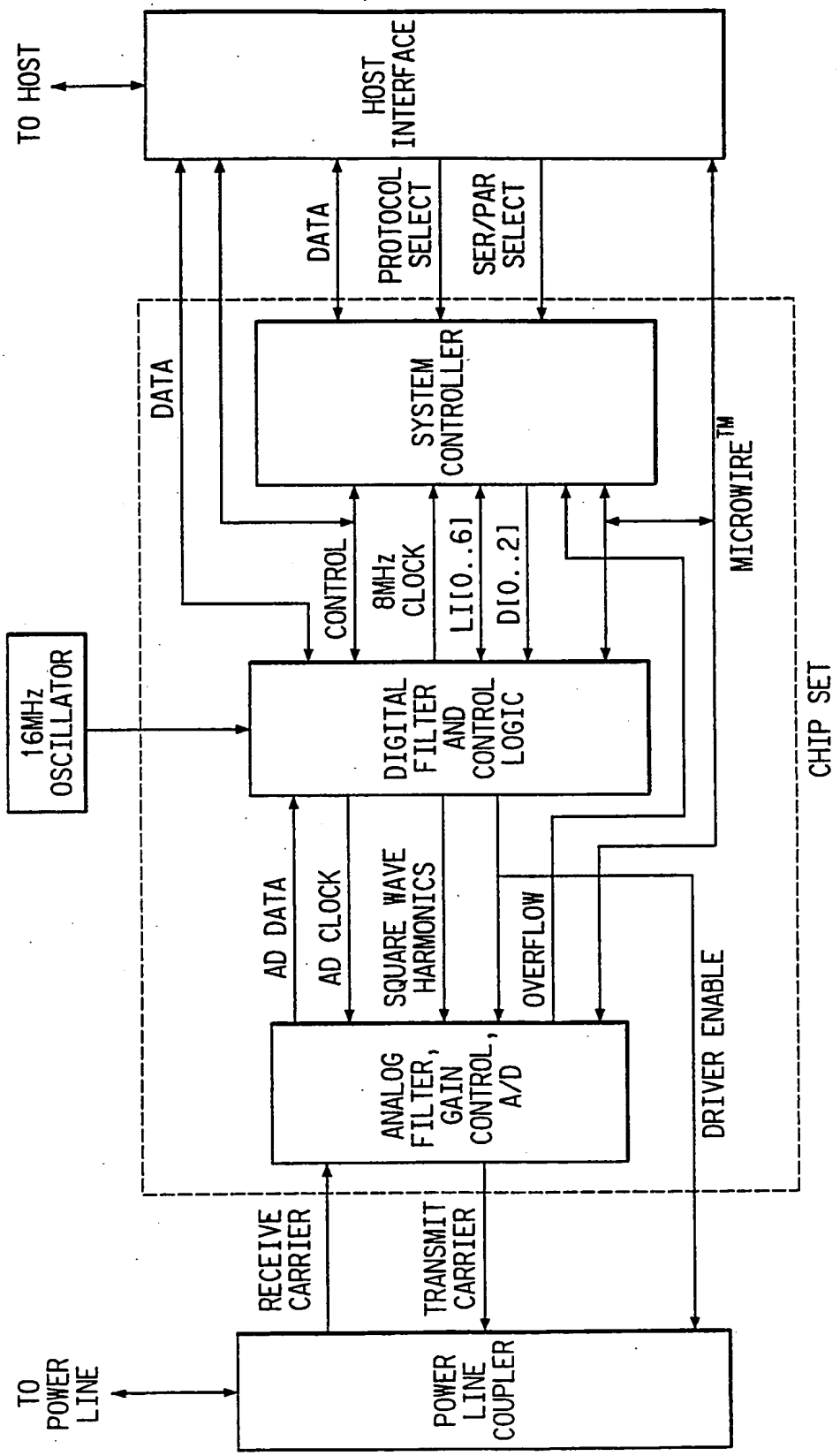
TO HOST
HOST INTERFACE
DATA
PROTOCOL SELECT
SER/PAR SELECT
DATA
SYSTEM CONTROLLER
MICROWIRE™
CONTROL
8MHz CLOCK
LI[0..6]
DI0..2]
16MHz OSCILLATOR
DIGITAL FILTER AND CONTROL LOGIC
CHIP SET
AD DATA
AD CLOCK
SQUARE WAVE HARMONICS
OVERFLOW
ANALOG FILTER, GAIN CONTROL, A/D
DRIVER ENABLE
RECEIVE CARRIER
TRANSMIT CARRIER
TO POWER LINE
POWER LINE COUPLER

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FIG.2

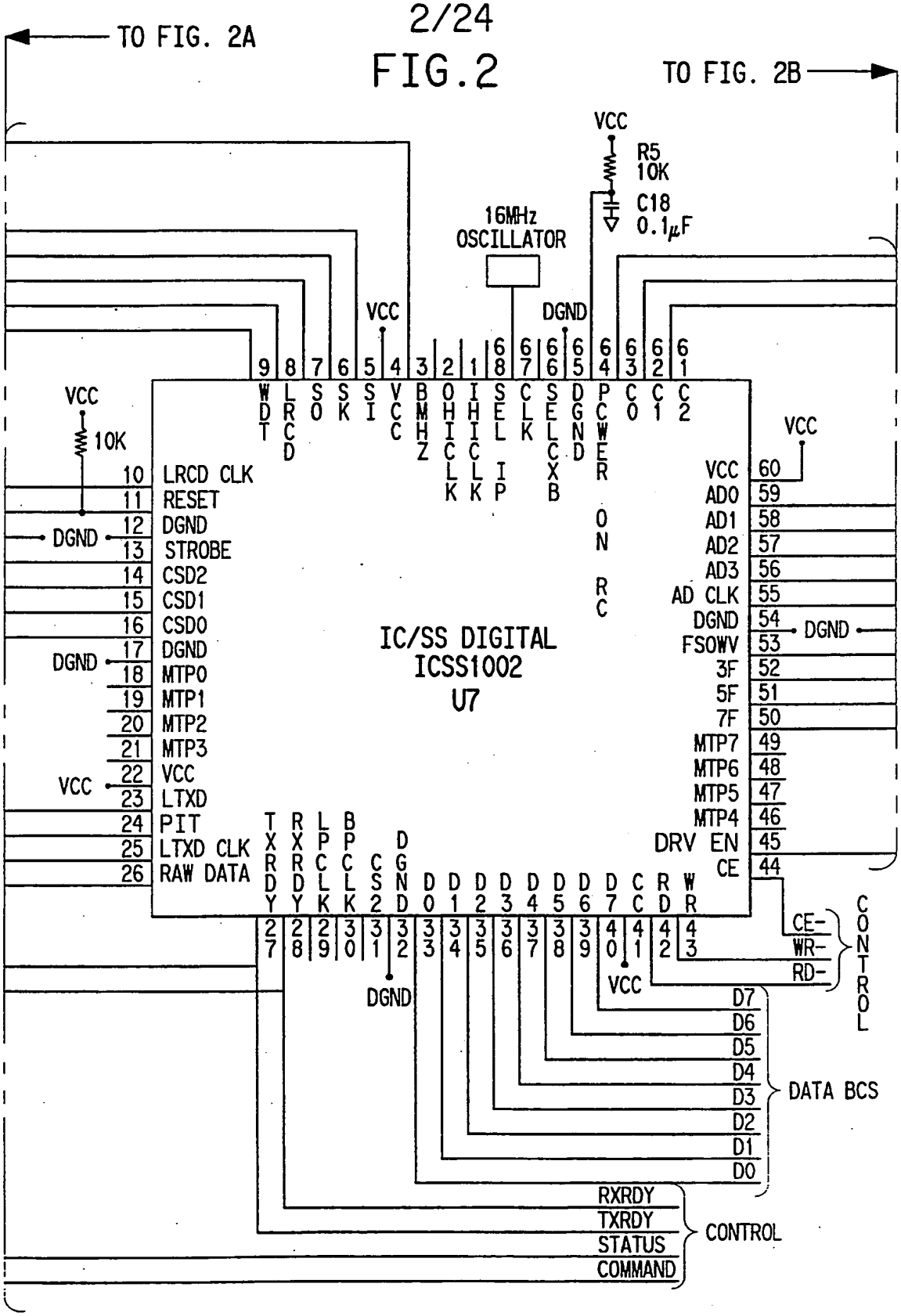
TO FIG. 2A
TO FIG. 2B
VCC
R5
10K
C18
0.1μF
16MHz
OSCILLATOR
VCC
DGND
10K
IC/SS DIGITAL
ICSS1002
U7
LRCD CLK
RESET
DGND
STROBE
CSD2
CSD1
CSD0
DGND
MTP0
MTP1
MTP2
MTP3
VCC
LTXD
PIT
LTXD CLK
RAW DATA
VCC
AD0
AD1
AD2
AD3
AD CLK
DGND
FSOWV
3F
5F
7F
MTP7
MTP6
MTP5
MTP4
DRV EN
CE
CE-
WR-
RD-
CONTROL
DATA BCS
D7
D6
D5
D4
D3
D2
D1
D0
RXRDY
TXRDY
STATUS
COMMAND
CONTROL

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FIG.2A

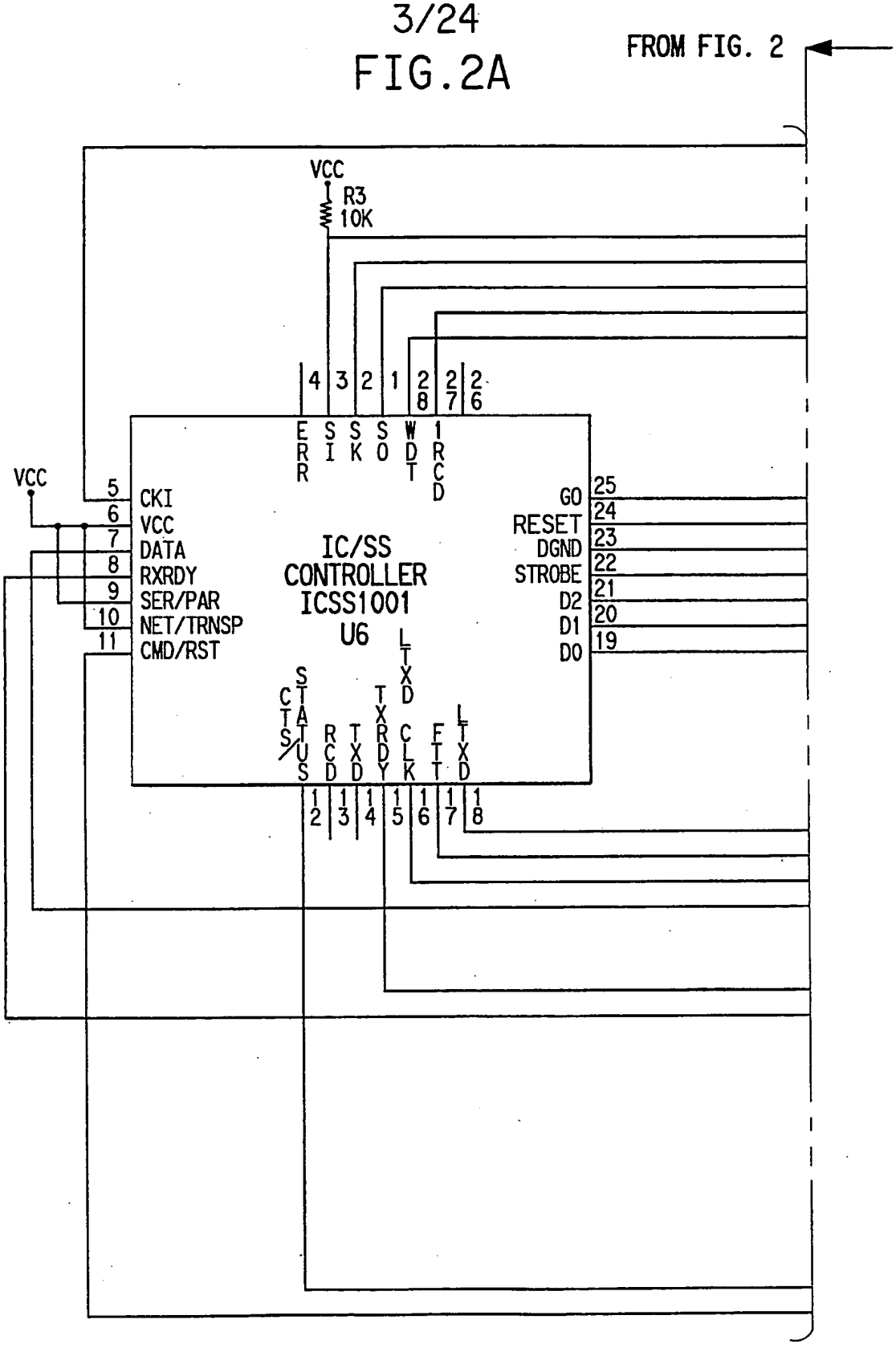
FROM FIG. 2
VCC
R3
10K
4 3 2 1 28 27 26
ERR SIK SKO SDO WDT IRCD
VCC
5 CKI
6 VCC
7 DATA
8 RXRDY
9 SER/PAR
10 NET/TRNSP
11 CMD/RST
IC/SS
CONTROLLER
ICSS1001
U6
25 GO
24 RESET
23 DGND
22 STROBE
21 D2
20 D1
19 D0
LTXD
CTS/STATUS RCD TXD TXRDY CLK FTT LTXD
12 13 14 15 16 17 18

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FIG.2B

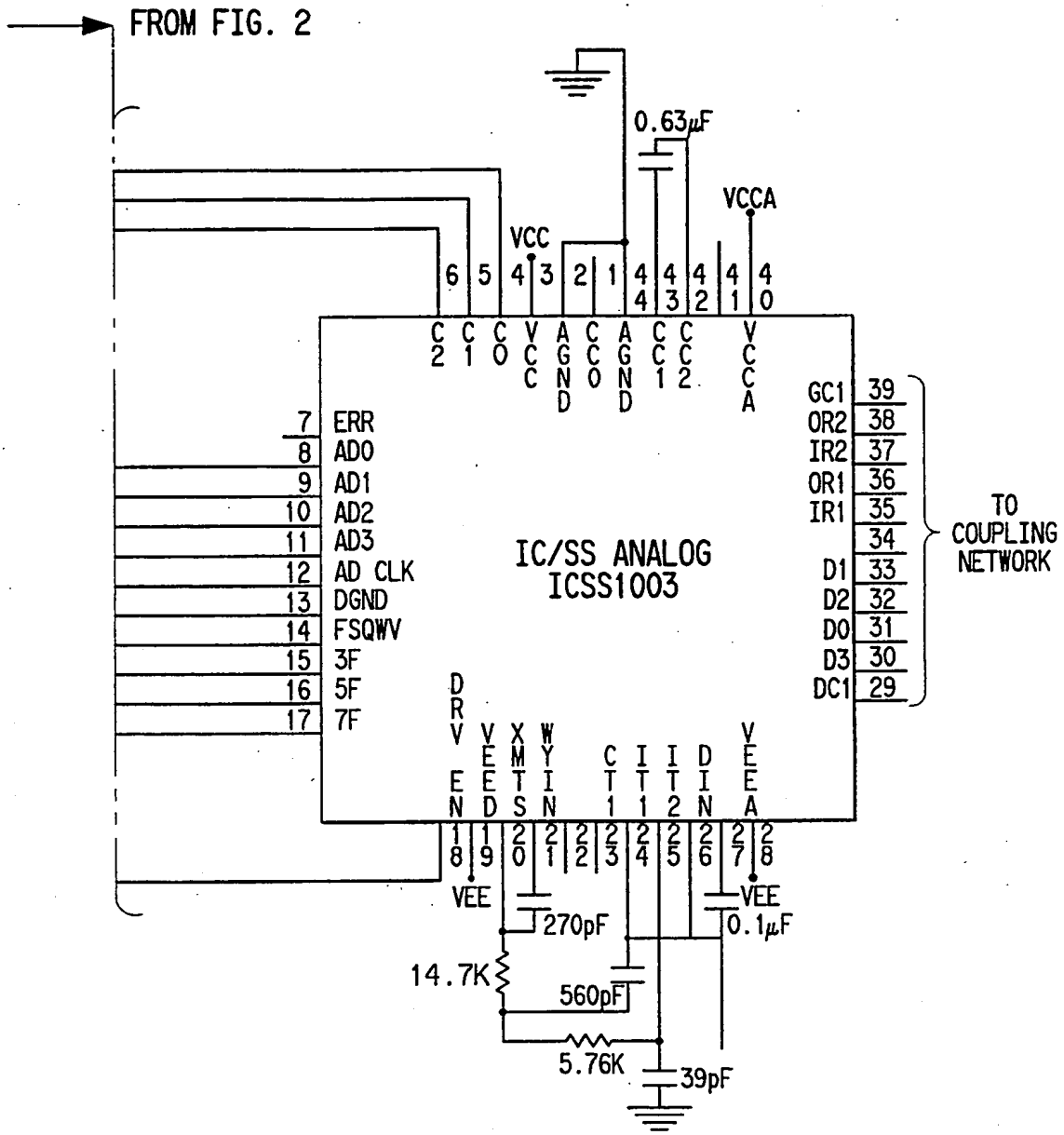
FROM FIG. 2
0.63μF
VCC
VCCA
IC/SS ANALOG
ICSS1003
TO
COUPLING
NETWORK
ERR
AD0
AD1
AD2
AD3
AD CLK
DGND
FSQWV
3F
5F
7F
GC1
OR2
IR2
OR1
IR1
D1
D2
D0
D3
DC1
VEE
270pF
0.1μF
14.7K
560pF
5.76K
39pF

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FIG.3

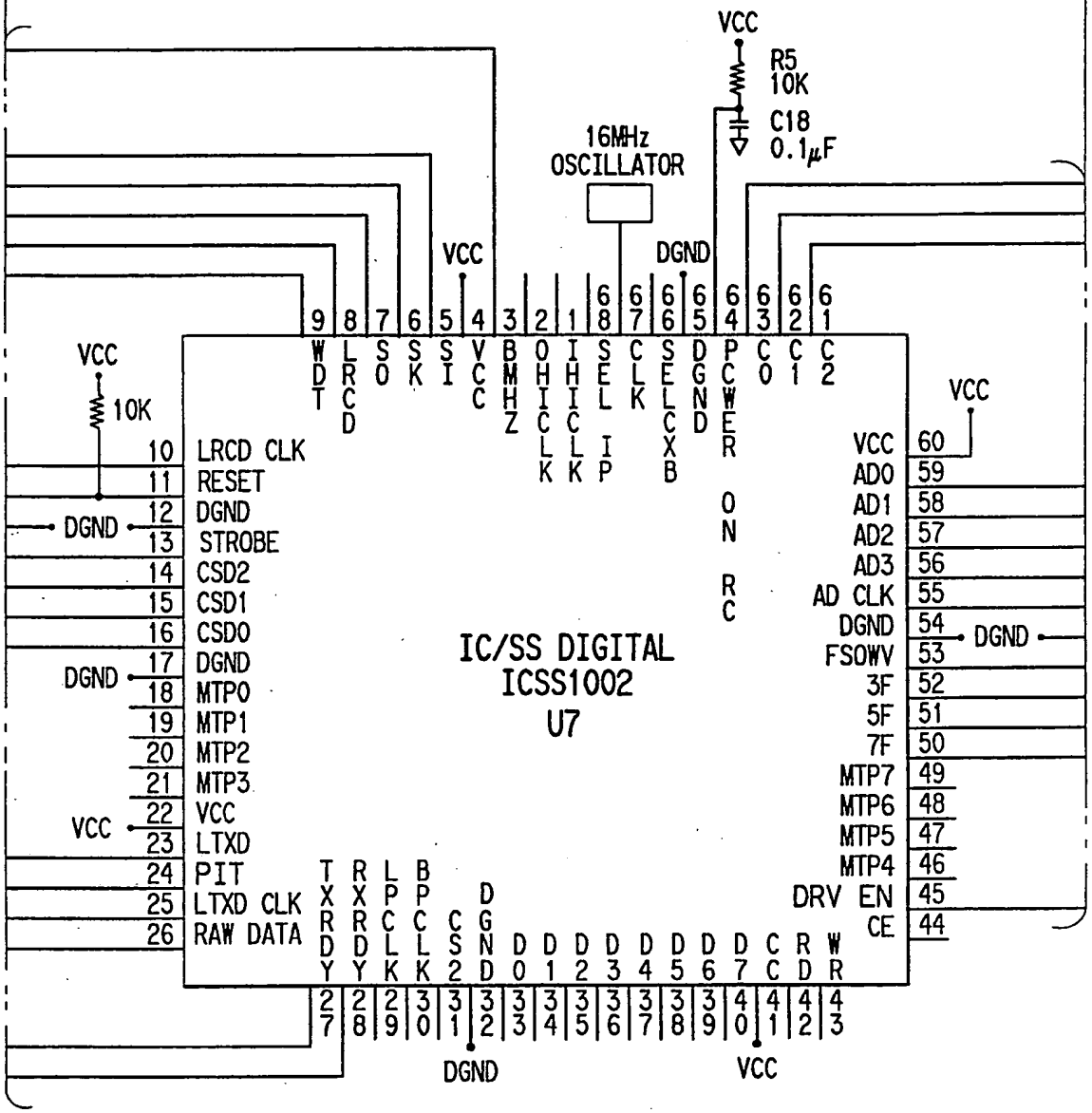
TO FIG. 3A
TO FIG. 3B
VCC
R5
10K
C18
0.1μF
16MHz
OSCILLATOR
DGND
VCC
10K
IC/SS DIGITAL
ICSS1002
U7
LRCD CLK
RESET
DGND
STROBE
CSD2
CSD1
CSD0
DGND
MTP0
MTP1
MTP2
MTP3
VCC
LTXD
PIT
LTXD CLK
RAW DATA
AD0
AD1
AD2
AD3
AD CLK
DGND
FSOWV
3F
5F
7F
MTP7
MTP6
MTP5
MTP4
DRV EN
CE
WDT
LRCD
SO
SK
SI
VCC
BMHZ
OHICLK
IHICLK
SEL IP
CLK
SELCXB
DGND
PCWER ON RC
C0
C1
C2
TXRDY
RXRDY
LPCLK
BPCLK
CS2
DGND
D0
D1
D2
D3
D4
D5
D6
D7
CC
RD
WR

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FIG.3A

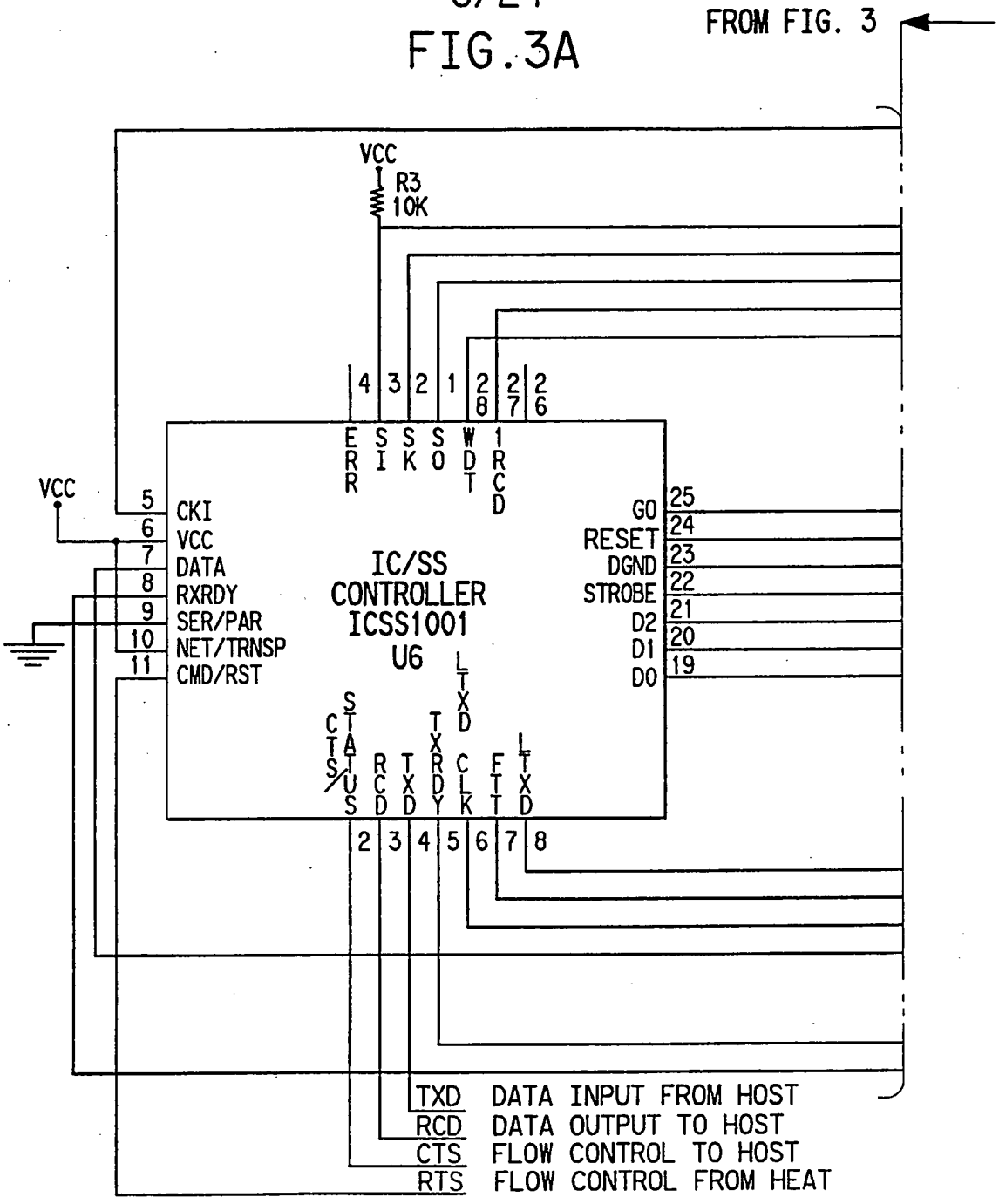
FROM FIG. 3
VCC
R3
10K
4 3 2 1 28 27 26
ERR SIK SKO SDT WDT 1RCD
VCC
5 CKI
6 VCC
7 DATA
8 RXRDY
9 SER/PAR
10 NET/TRNSP
11 CMD/RST
IC/SS
CONTROLLER
ICSS1001
U6
25 GO
24 RESET
23 DGND
22 STROBE
21 D2
20 D1
19 D0
CTS/STATUS RCD TXD TXRDY CLK FTT LTXD
2 3 4 5 6 7 8
TXD DATA INPUT FROM HOST
RCD DATA OUTPUT TO HOST
CTS FLOW CONTROL TO HOST
RTS FLOW CONTROL FROM HEAT

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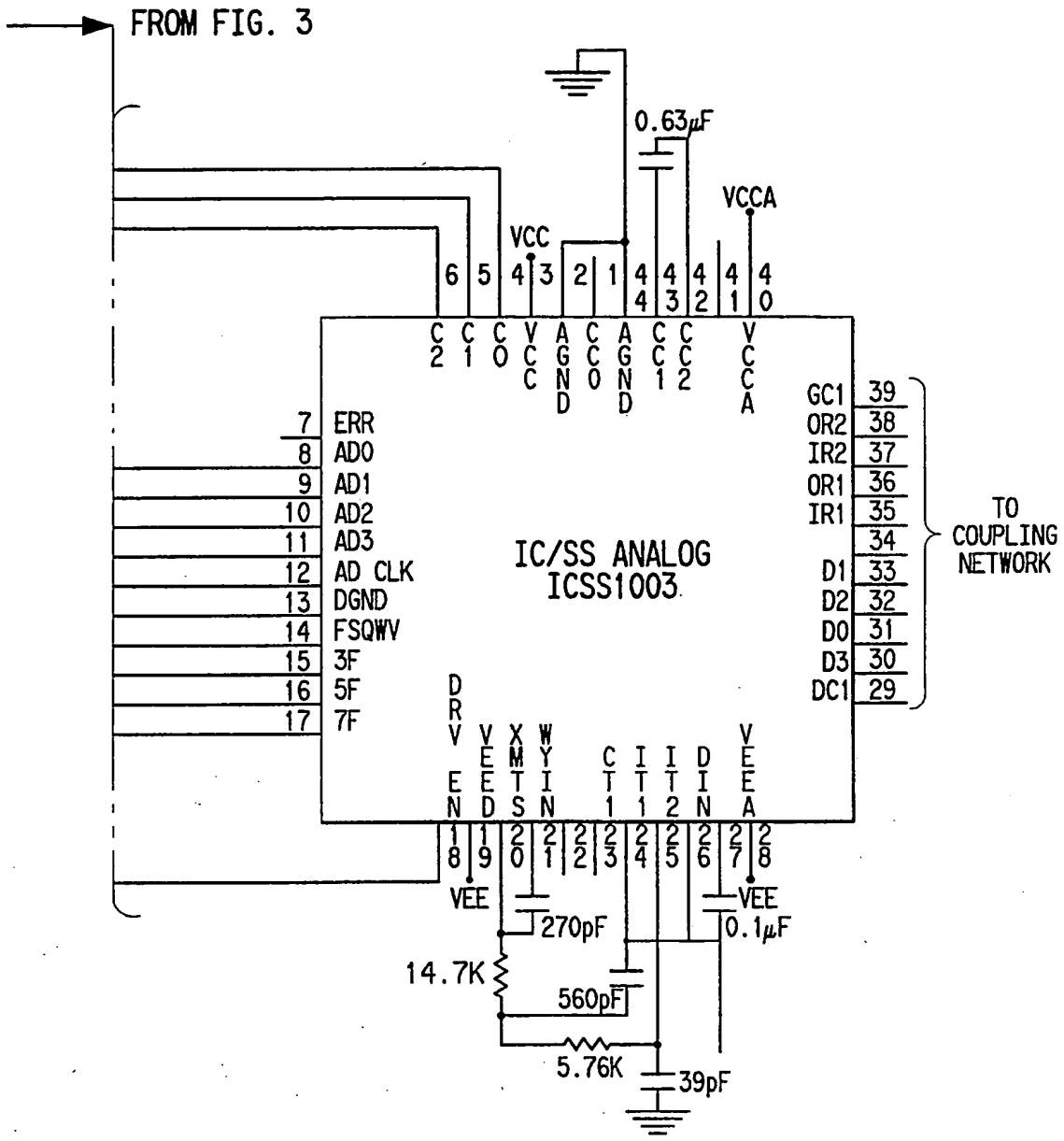
FIG.3B


FROM FIG. 3
0.63μF
VCCA
VCC
6 5 4 3 2 1 44 43 42 41 40
C21 C10 VCC AGND CC0 AGND CC1 CC2 VCCA
7 ERR
8 AD0
9 AD1
10 AD2
11 AD3
12 AD CLK
13 DGND
14 FSQWV
15 3F
16 5F
17 7F
IC/SS ANALOG
ICSS1003
GC1 39
OR2 38
IR2 37
OR1 36
IR1 35
34
D1 33
D2 32
D0 31
D3 30
DC1 29
TO COUPLING NETWORK
DRV EN 18
VEE D 19
XMTS 20
WYIN 21
22
CT1 23
IT1 24
IT2 25
DIN 26
VEE A 27
28
VEE
270pF
0.1μF
14.7K
560pF
5.76K
39pF

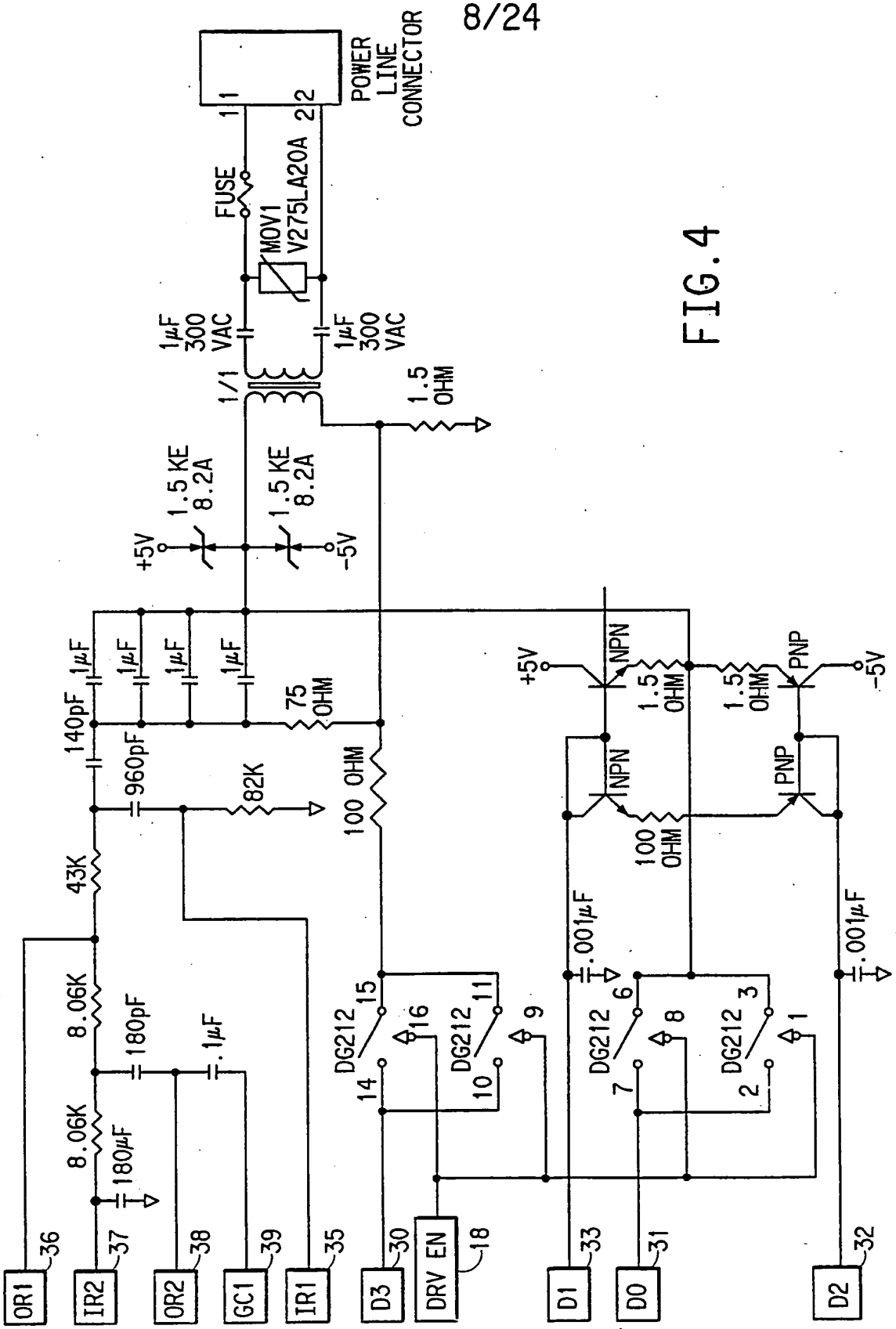

POWER LINE CONNECTOR
1
2
FUSE
MOV1 V275LA20A
1μF 300 VAC
1μF 300 VAC
1/1
1.5 OHM
1.5 KE 8.2A
1.5 KE 8.2A
+5V
-5V
1μF
140pF
960pF
82K
75 OHM
100 OHM
43K
8.06K
180pF
180μF
.1μF
NPN
PNP
.001μF
DG212
OR1
IR2
OR2
GC1
IR1
D3
DRV EN
D1
D0
D2

FIG. 4

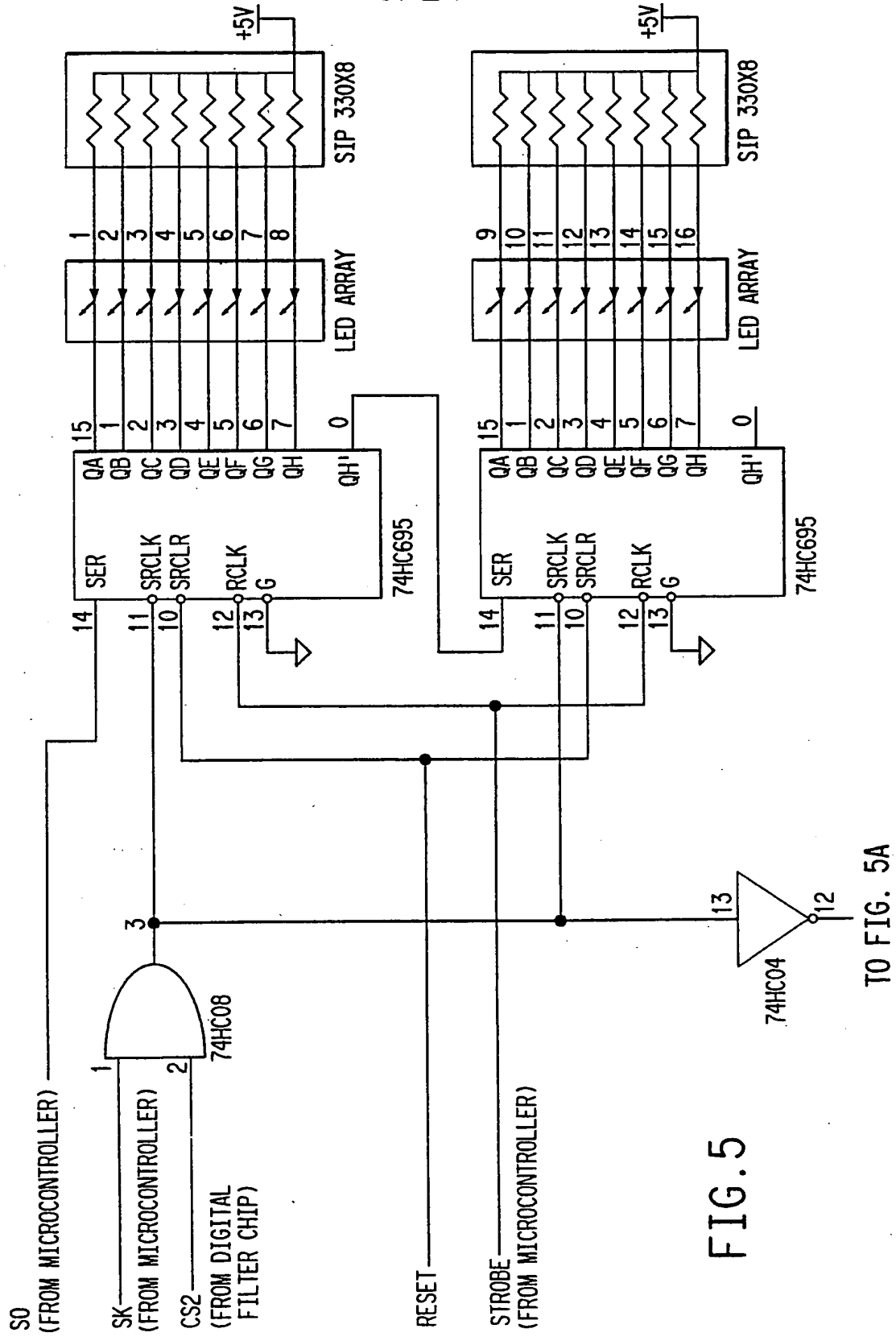

+5V
SIP 330X8
LED ARRAY
74HC695
SER
SRCLK
SRCLR
RCLK
G
QA
QB
QC
QD
QE
QF
QG
QH
QH'
74HC08
74HC04
SO
(FROM MICROCONTROLLER)
SK
(FROM MICROCONTROLLER)
CS2
(FROM DIGITAL
FILTER CHIP)
RESET
STROBE
(FROM MICROCONTROLLER)
TO FIG. 5A

FIG.5

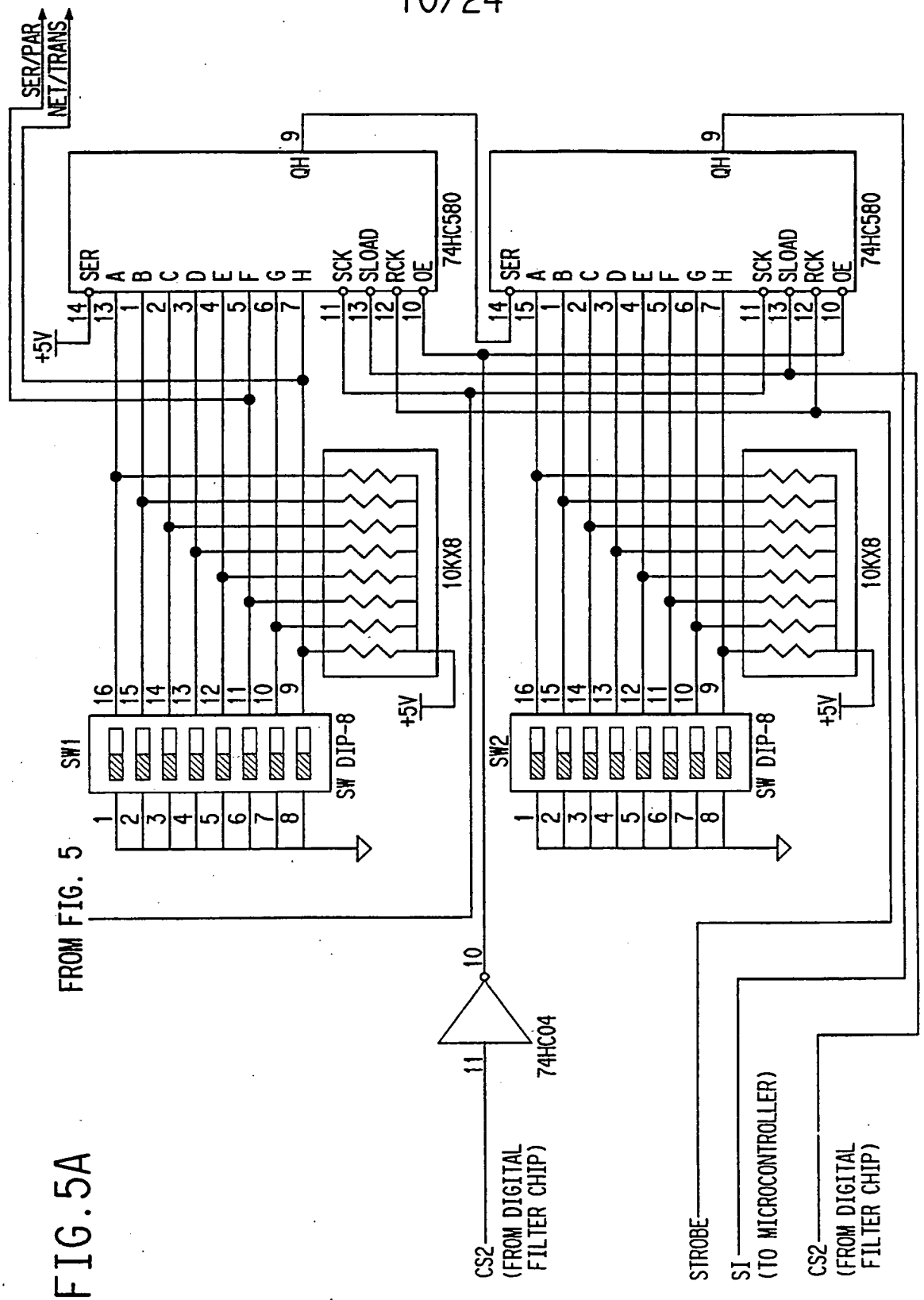

SER/PAR
NET/TRANS
74HC580
SER
A
B
C
D
E
F
G
H
SCK
SLOAD
RCK
OE
QH
+5V
10KX8
SW1
SW2
SW DIP-8
FROM FIG. 5
74HC04
CS2
(FROM DIGITAL
FILTER CHIP)
STROBE
SI
(TO MICROCONTROLLER)

FIG.5A

FIG.6

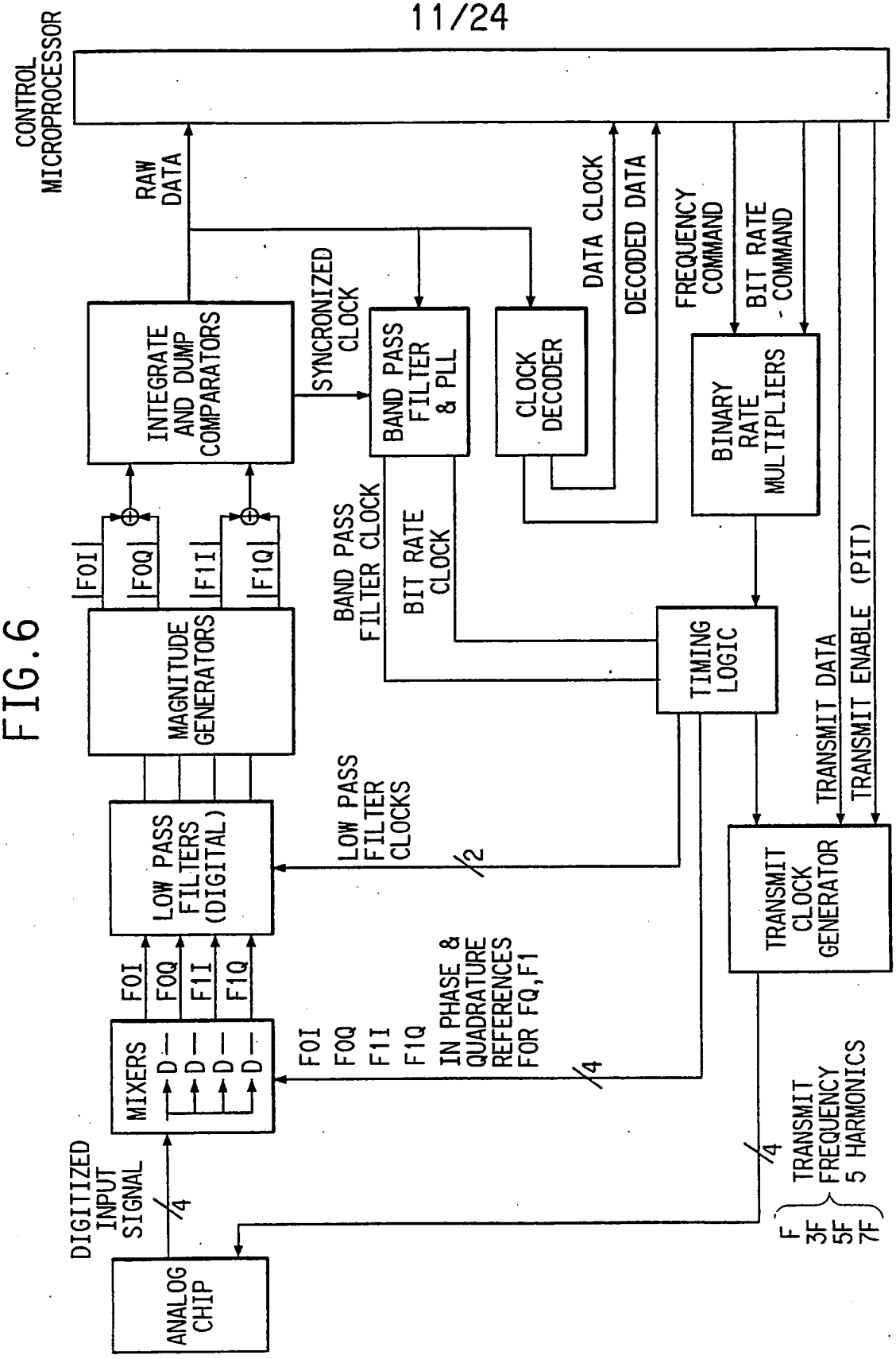
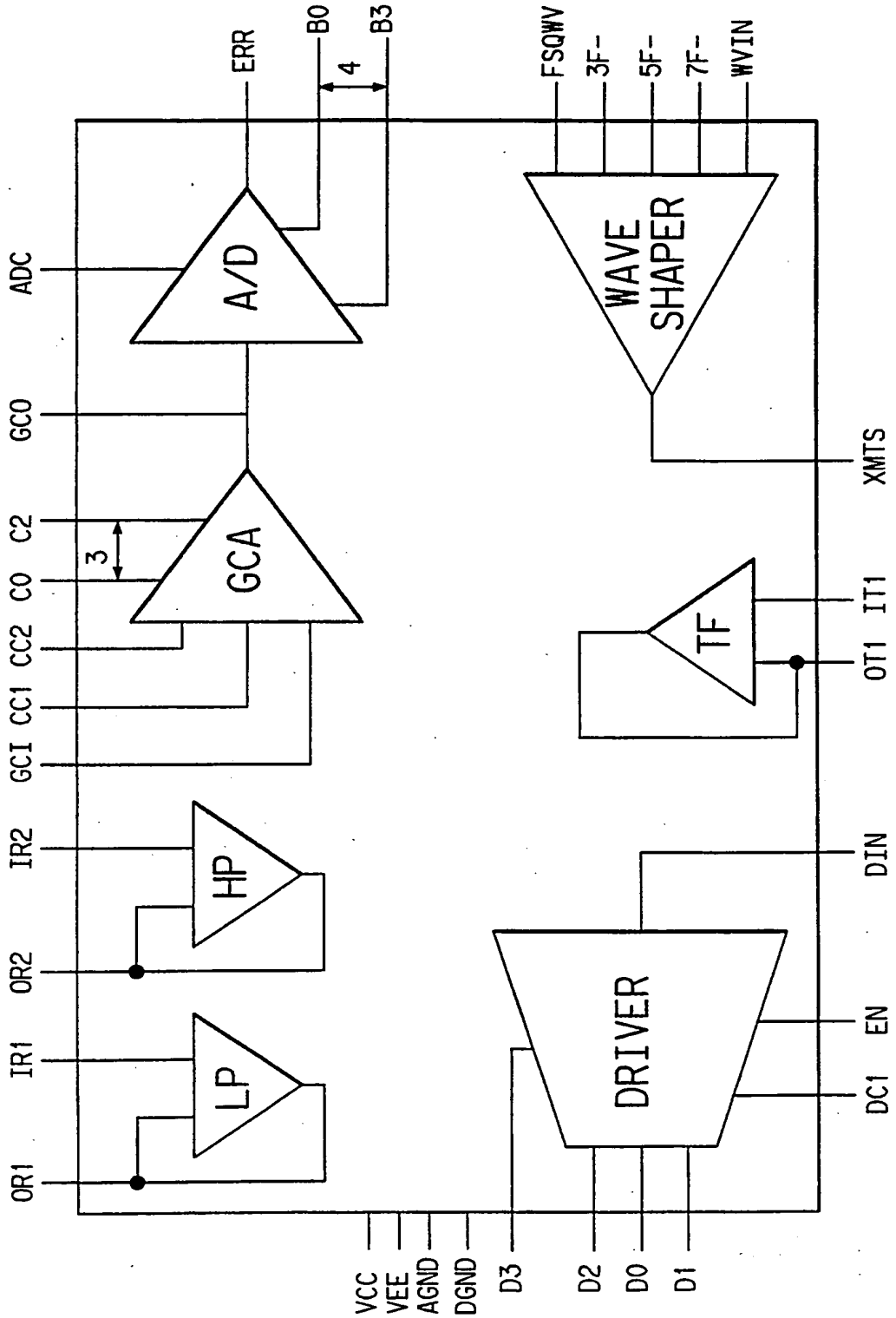

CONTROL MICROPROCESSOR
RAW DATA
INTEGRATE AND DUMP COMPARATORS
SYNCRONIZED CLOCK
BAND PASS FILTER & PLL
CLOCK DECODER
DATA CLOCK
DECODED DATA
FREQUENCY COMMAND
BIT RATE - COMMAND
BINARY RATE MULTIPLIERS
F0I
F0Q
F1I
F1Q
MAGNITUDE GENERATORS
BAND PASS FILTER CLOCK
BIT RATE CLOCK
TIMING LOGIC
TRANSMIT DATA
TRANSMIT ENABLE (PIT)
LOW PASS FILTERS (DIGITAL)
LOW PASS FILTER CLOCKS
/2
TRANSMIT CLOCK GENERATOR
MIXERS
D
F0I
F0Q
F1I
F1Q
IN PHASE & QUADRATURE REFERENCES FOR FQ,F1
/4
DIGITIZED INPUT SIGNAL
/4
ANALOG CHIP
/4
TRANSMIT FREQUENCY 5 HARMONICS
F
3F
5F
7F

FIG.7


ERR
B0
B3
4
FSQWV
3F-
5F-
7F-
WVIN
A/D
WAVE SHAPER
ADC
GCO
C2
C0
3
GCA
CC2
CC1
GCI
XMTS
TF
IT1
OT1
IR2
HP
OR2
DIN
IR1
LP
DRIVER
EN
DC1
OR1
VCC
VEE
AGND
DGND
D3
D2
D0
D1

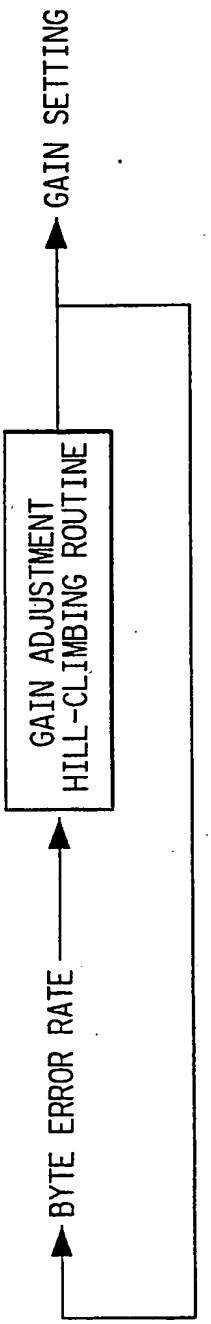

GAIN SETTING
GAIN ADJUSTMENT HILL-CLIMBING ROUTINE
BYTE ERROR RATE

FIG.8A

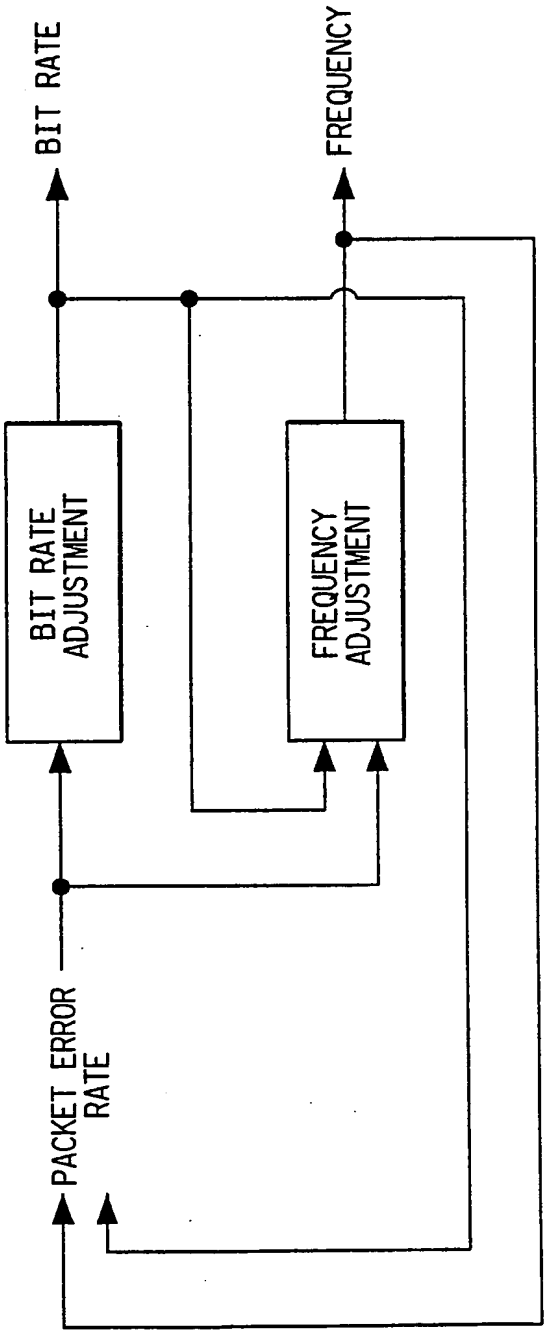

BIT RATE
FREQUENCY
BIT RATE ADJUSTMENT
FREQUENCY ADJUSTMENT
PACKET ERROR RATE

FIG.8B

FIG.9

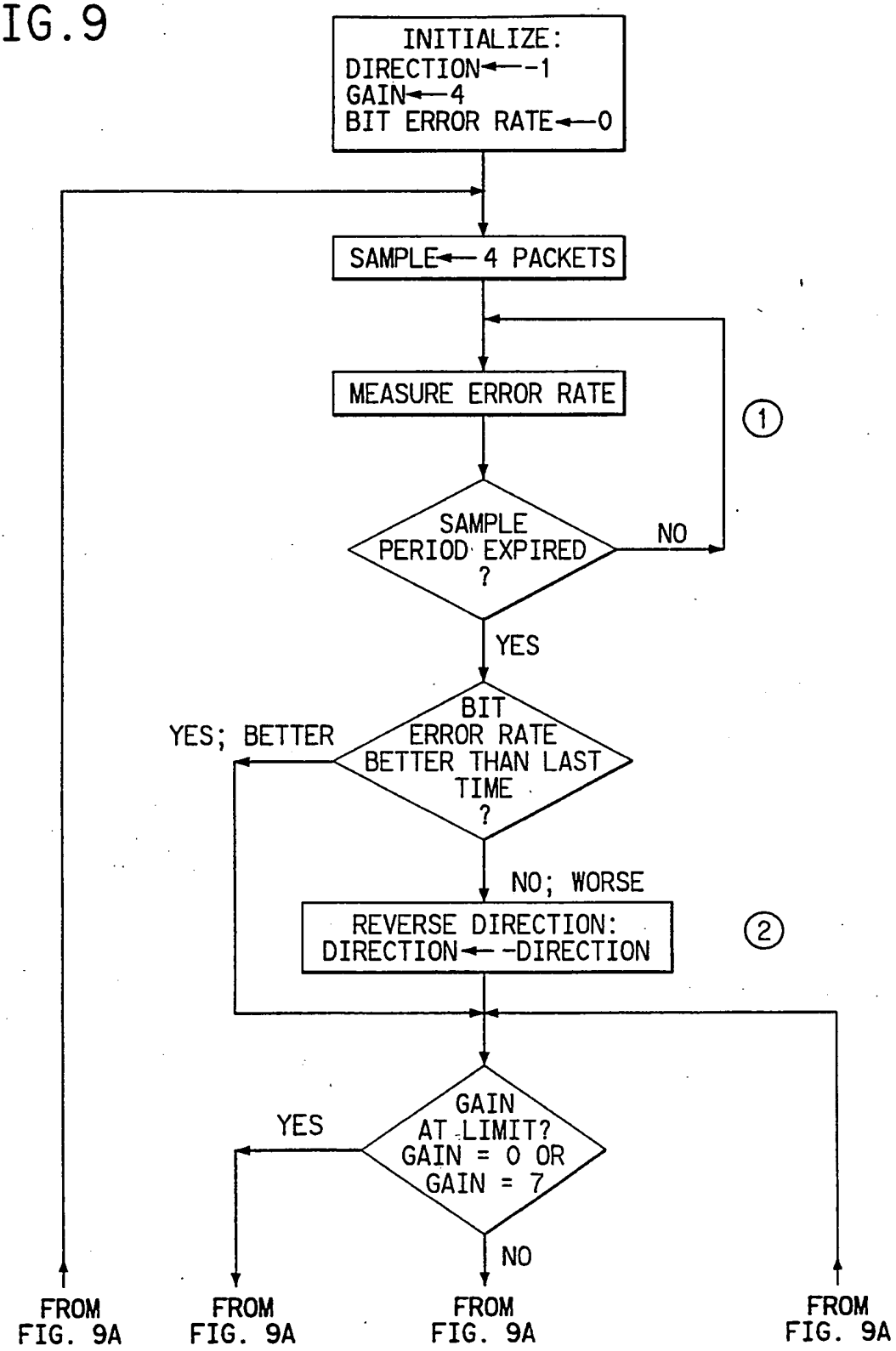

INITIALIZE:
DIRECTION←-1
GAIN←4
BIT ERROR RATE←0
SAMPLE←4 PACKETS
MEASURE ERROR RATE
1
SAMPLE PERIOD EXPIRED ?
NO
YES
BIT ERROR RATE BETTER THAN LAST TIME ?
YES; BETTER
NO; WORSE
REVERSE DIRECTION:
DIRECTION←-DIRECTION
2
GAIN AT LIMIT? GAIN = 0 OR GAIN = 7
YES
NO
FROM FIG. 9A
FROM FIG. 9A
FROM FIG. 9A
FROM FIG. 9A

FIG. 9A

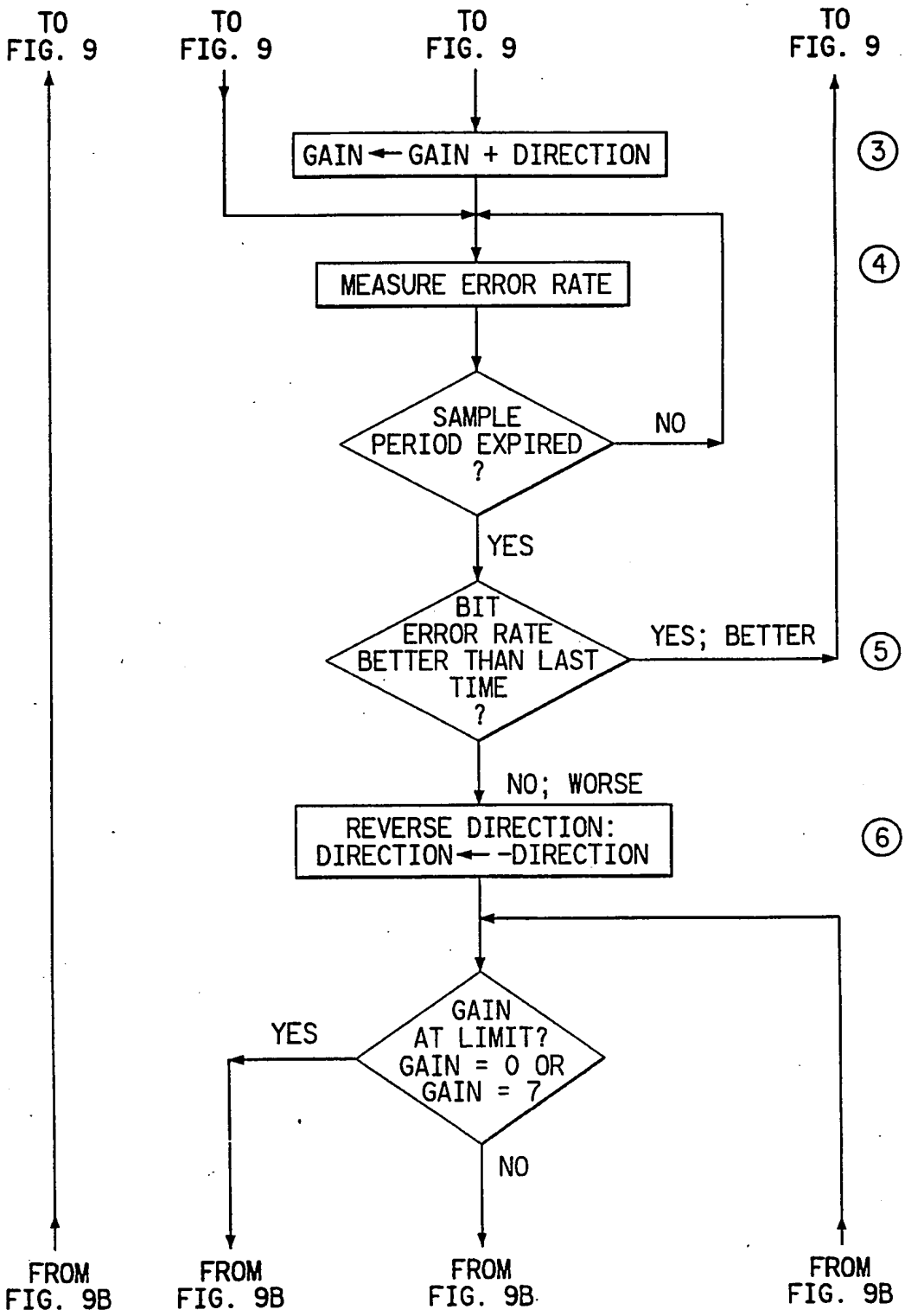
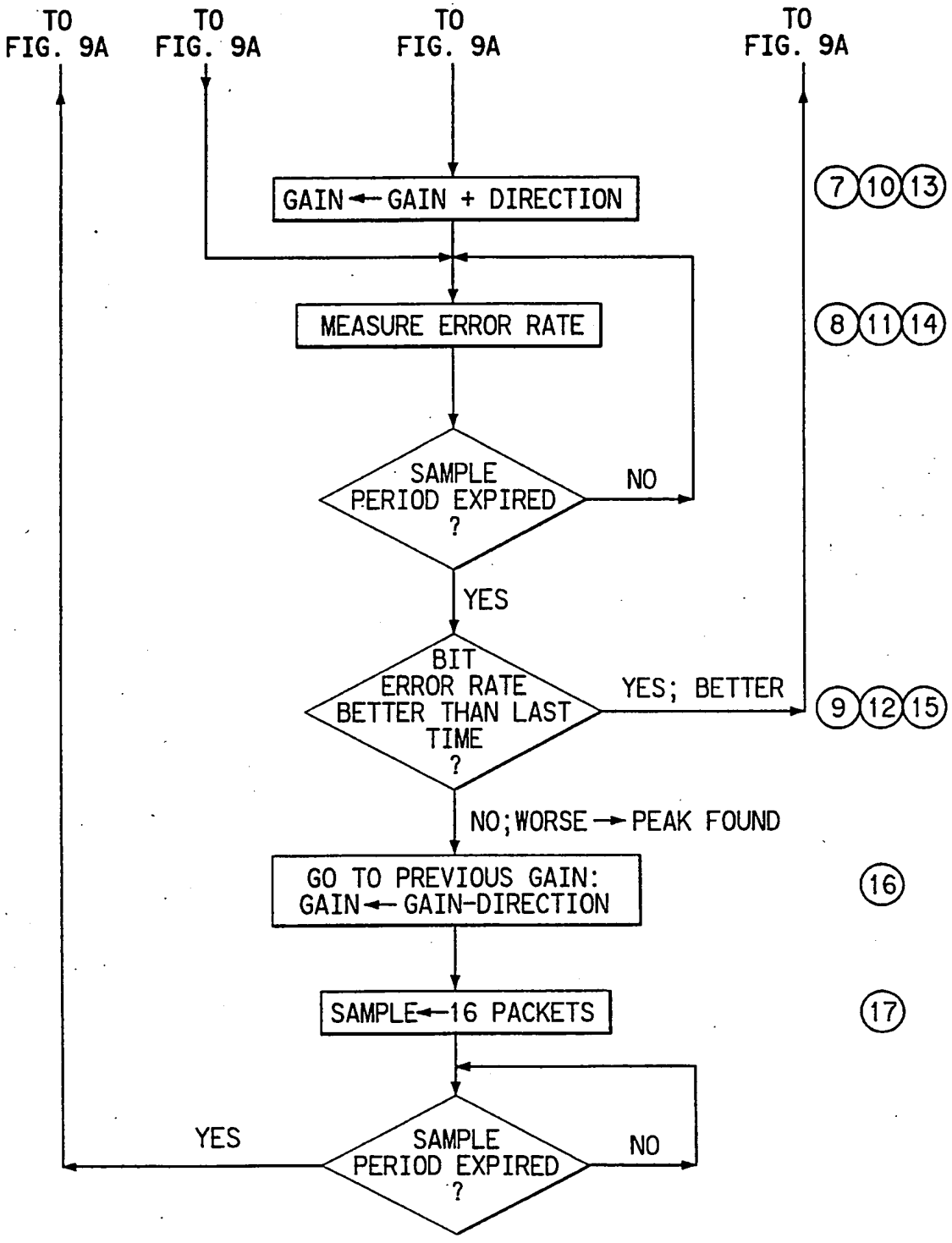

TO FIG. 9
TO FIG. 9
TO FIG. 9
TO FIG. 9
GAIN ← GAIN + DIRECTION
3
MEASURE ERROR RATE
4
SAMPLE PERIOD EXPIRED ?
NO
YES
BIT ERROR RATE BETTER THAN LAST TIME ?
YES; BETTER
5
NO; WORSE
REVERSE DIRECTION: DIRECTION ← -DIRECTION
6
GAIN AT LIMIT? GAIN = 0 OR GAIN = 7
YES
NO
FROM FIG. 9B
FROM FIG. 9B
FROM FIG. 9B
FROM FIG. 9B

FIG. 9B


TO FIG. 9A
TO FIG. 9A
TO FIG. 9A
TO FIG. 9A
GAIN ← GAIN + DIRECTION
7 10 13
MEASURE ERROR RATE
8 11 14
SAMPLE PERIOD EXPIRED ?
NO
YES
BIT ERROR RATE BETTER THAN LAST TIME ?
YES; BETTER
9 12 15
NO; WORSE → PEAK FOUND
GO TO PREVIOUS GAIN: GAIN ← GAIN-DIRECTION
16
SAMPLE ← 16 PACKETS
17
SAMPLE PERIOD EXPIRED ?
YES
NO

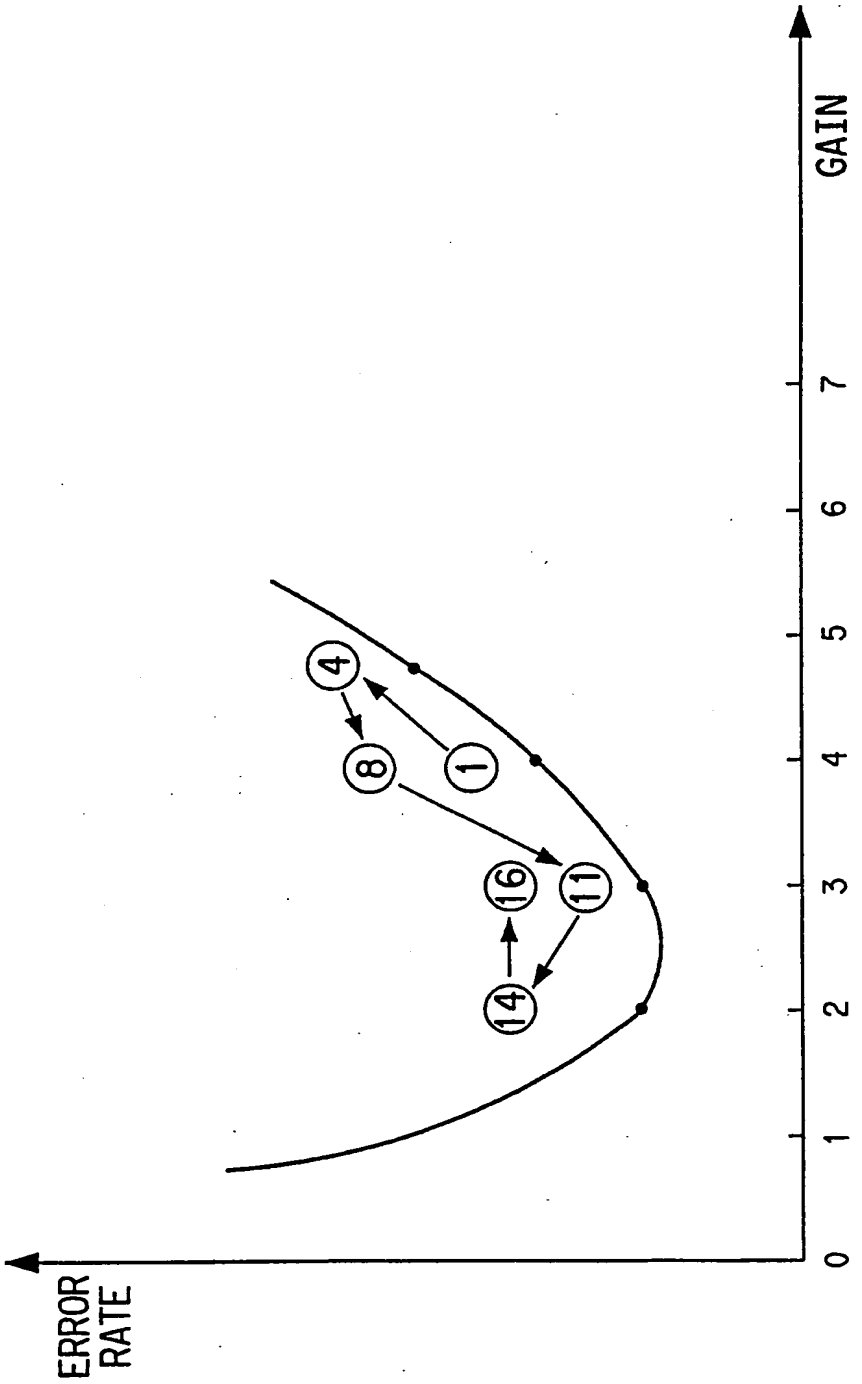


FIG.10

FIG.11

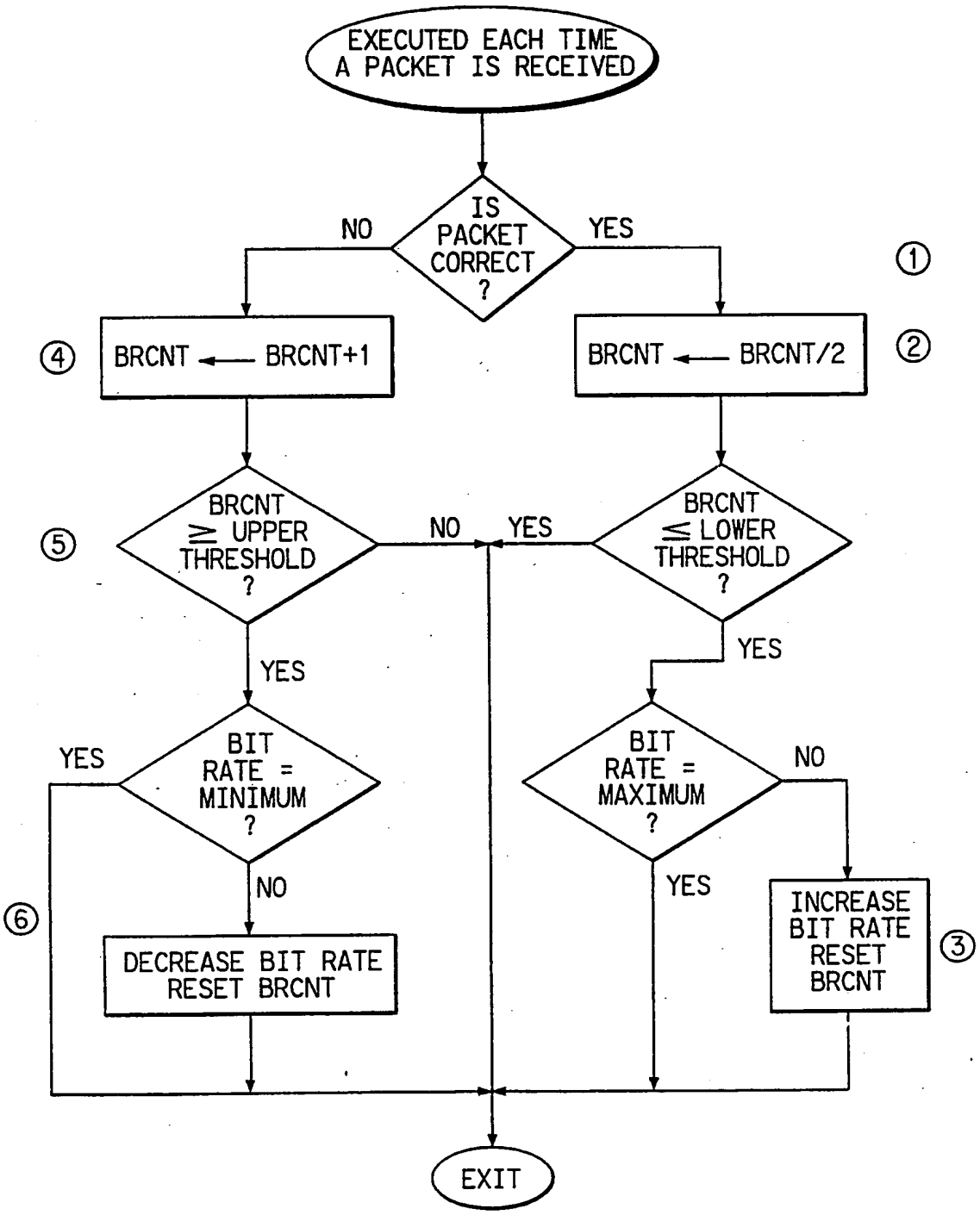
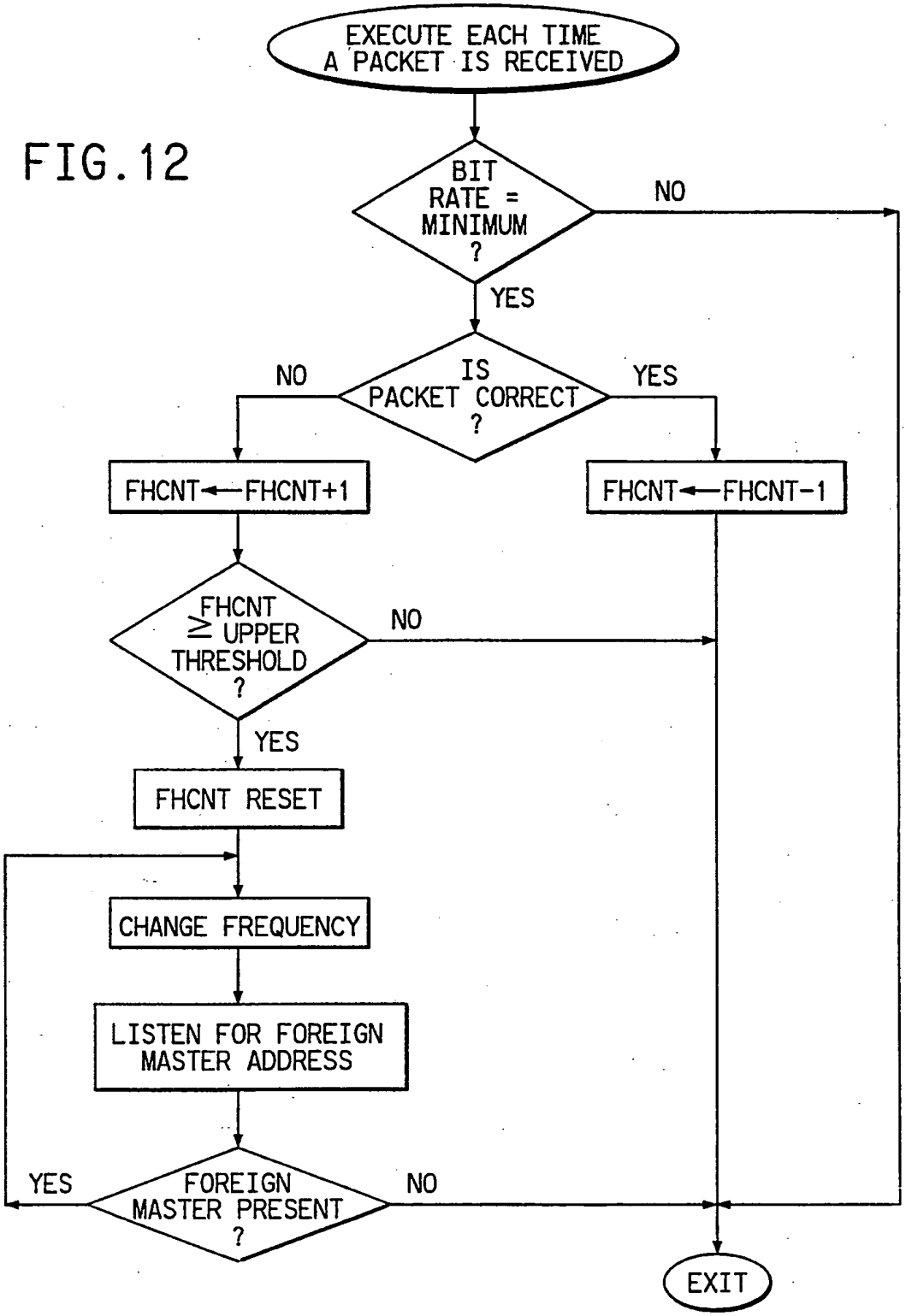

EXECUTED EACH TIME A PACKET IS RECEIVED
IS PACKET CORRECT ?
NO
YES
①
④
BRCNT ← BRCNT+1
BRCNT ← BRCNT/2
②
⑤
BRCNT ≧ UPPER THRESHOLD ?
NO
YES
BRCNT ≦ LOWER THRESHOLD ?
YES
YES
BIT RATE = MINIMUM ?
YES
BIT RATE = MAXIMUM ?
NO
NO
YES
⑥
DECREASE BIT RATE RESET BRCNT
INCREASE BIT RATE RESET BRCNT
③
EXIT

FIG.12


EXECUTE EACH TIME A PACKET IS RECEIVED
BIT RATE = MINIMUM ?
NO
YES
IS PACKET CORRECT ?
NO
YES
FHCNT←FHCNT+1
FHCNT←FHCNT-1
FHCNT ≥ UPPER THRESHOLD ?
NO
YES
FHCNT RESET
CHANGE FREQUENCY
LISTEN FOR FOREIGN MASTER ADDRESS
YES
FOREIGN MASTER PRESENT ?
NO
EXIT

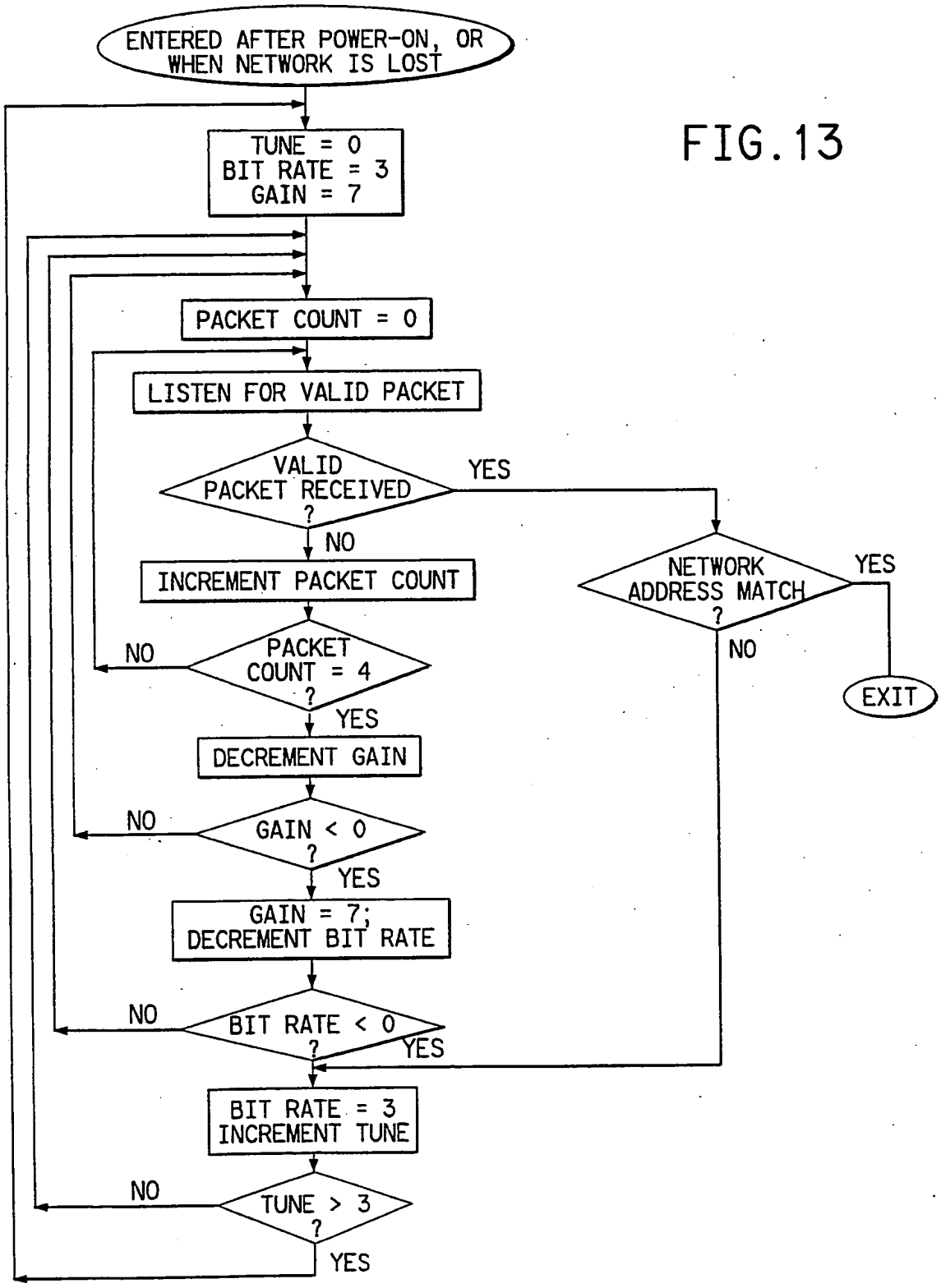

ENTERED AFTER POWER-ON, OR WHEN NETWORK IS LOST
TUNE = 0
BIT RATE = 3
GAIN = 7
PACKET COUNT = 0
LISTEN FOR VALID PACKET
VALID PACKET RECEIVED ?
YES
NO
INCREMENT PACKET COUNT
PACKET COUNT = 4 ?
NO
YES
DECREMENT GAIN
GAIN < 0 ?
NO
YES
GAIN = 7; DECREMENT BIT RATE
BIT RATE < 0 ?
NO
YES
BIT RATE = 3
INCREMENT TUNE
TUNE > 3 ?
NO
YES
NETWORK ADDRESS MATCH ?
YES
NO
EXIT

FIG.13

FIG.14

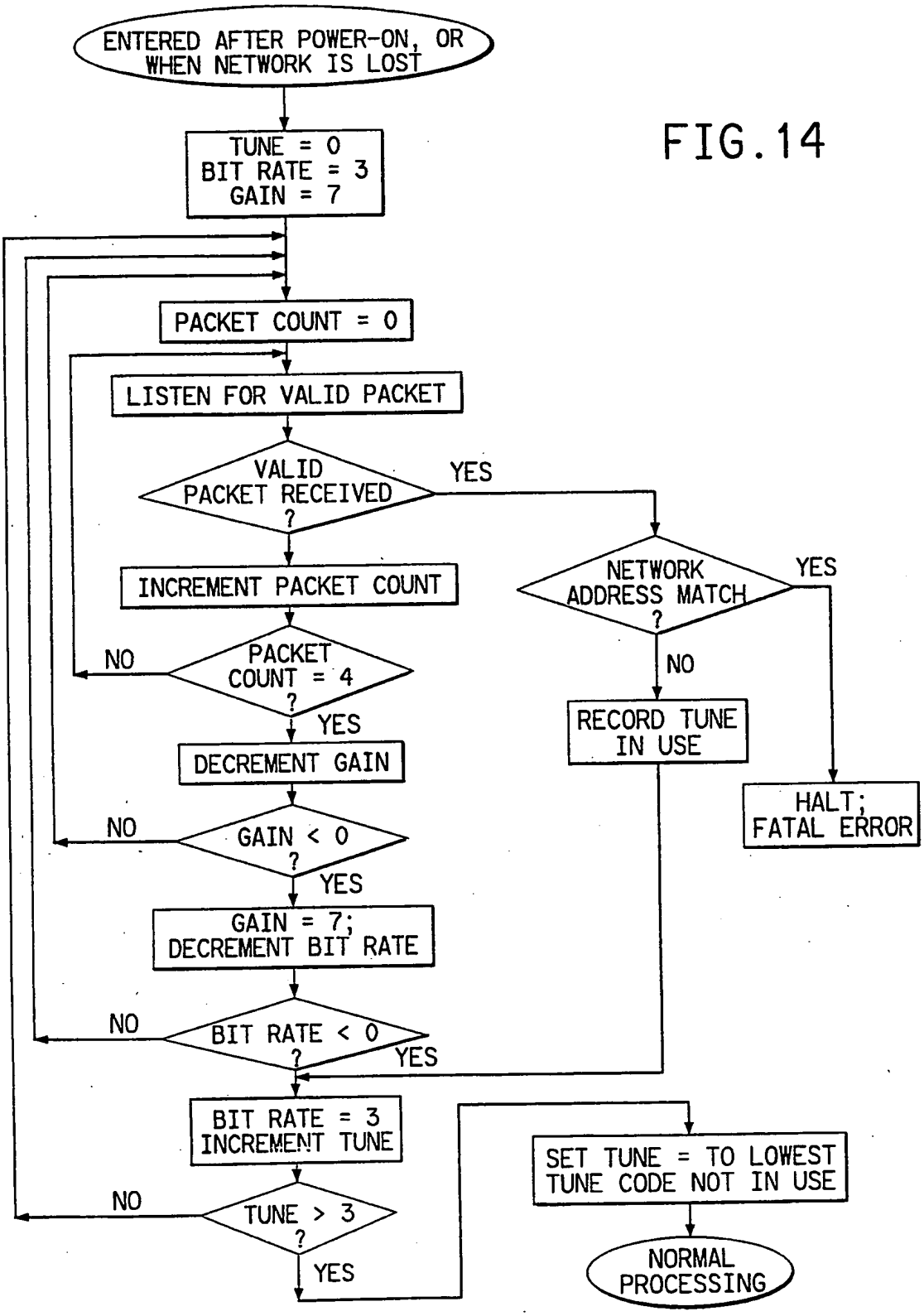

ENTERED AFTER POWER-ON, OR WHEN NETWORK IS LOST
TUNE = 0
BIT RATE = 3
GAIN = 7
PACKET COUNT = 0
LISTEN FOR VALID PACKET
VALID PACKET RECEIVED ?
YES
NO
INCREMENT PACKET COUNT
PACKET COUNT = 4 ?
NO
YES
DECREMENT GAIN
GAIN < 0 ?
NO
YES
GAIN = 7; DECREMENT BIT RATE
BIT RATE < 0 ?
NO
YES
BIT RATE = 3
INCREMENT TUNE
TUNE > 3 ?
NO
YES
NETWORK ADDRESS MATCH ?
YES
NO
RECORD TUNE IN USE
HALT; FATAL ERROR
SET TUNE = TO LOWEST TUNE CODE NOT IN USE
NORMAL PROCESSING

FIG. 15

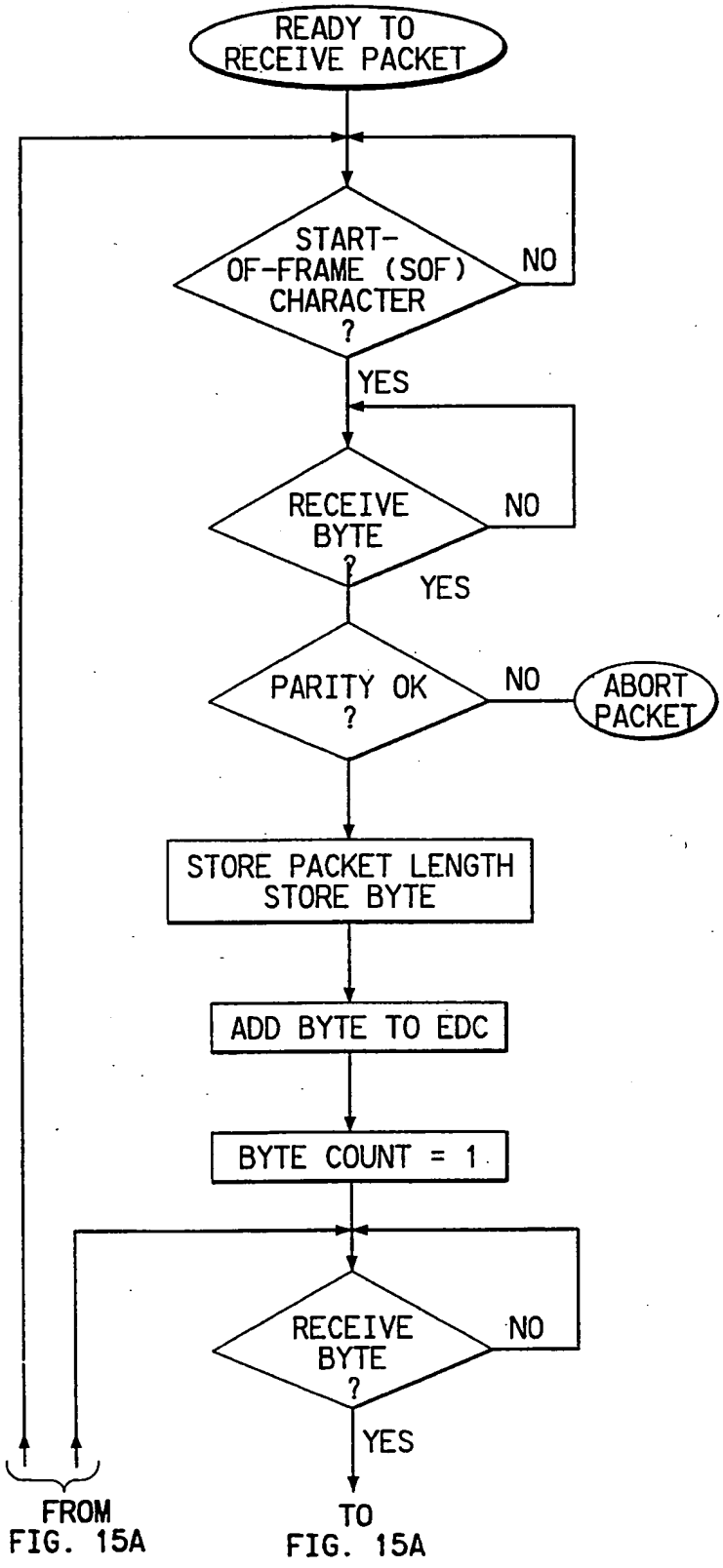

READY TO RECEIVE PACKET
START-OF-FRAME (SOF) CHARACTER ?
NO
YES
RECEIVE BYTE ?
NO
YES
PARITY OK ?
NO
ABORT PACKET
STORE PACKET LENGTH STORE BYTE
ADD BYTE TO EDC
BYTE COUNT = 1
RECEIVE BYTE ?
NO
YES
FROM FIG. 15A
TO FIG. 15A

FIG.15A

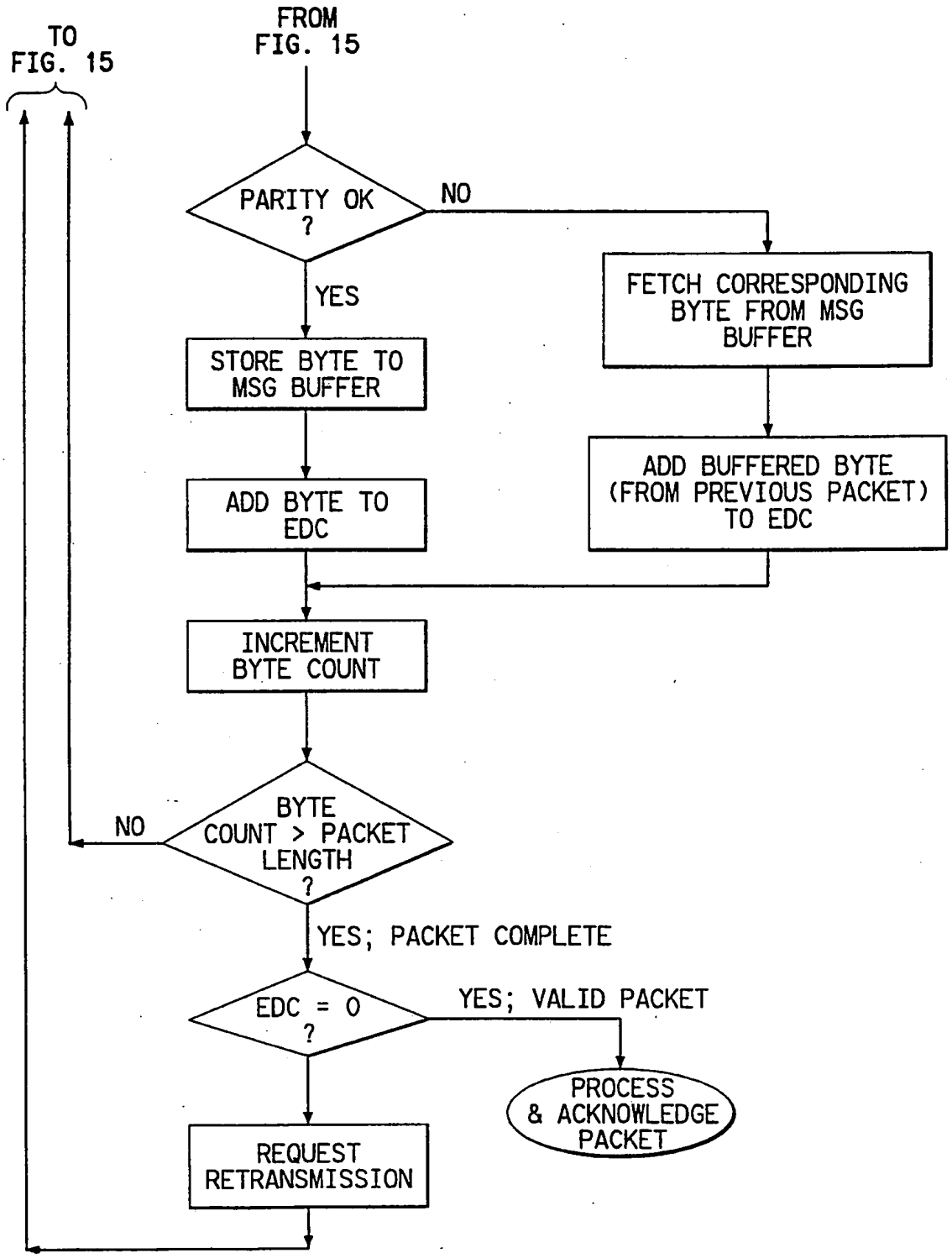
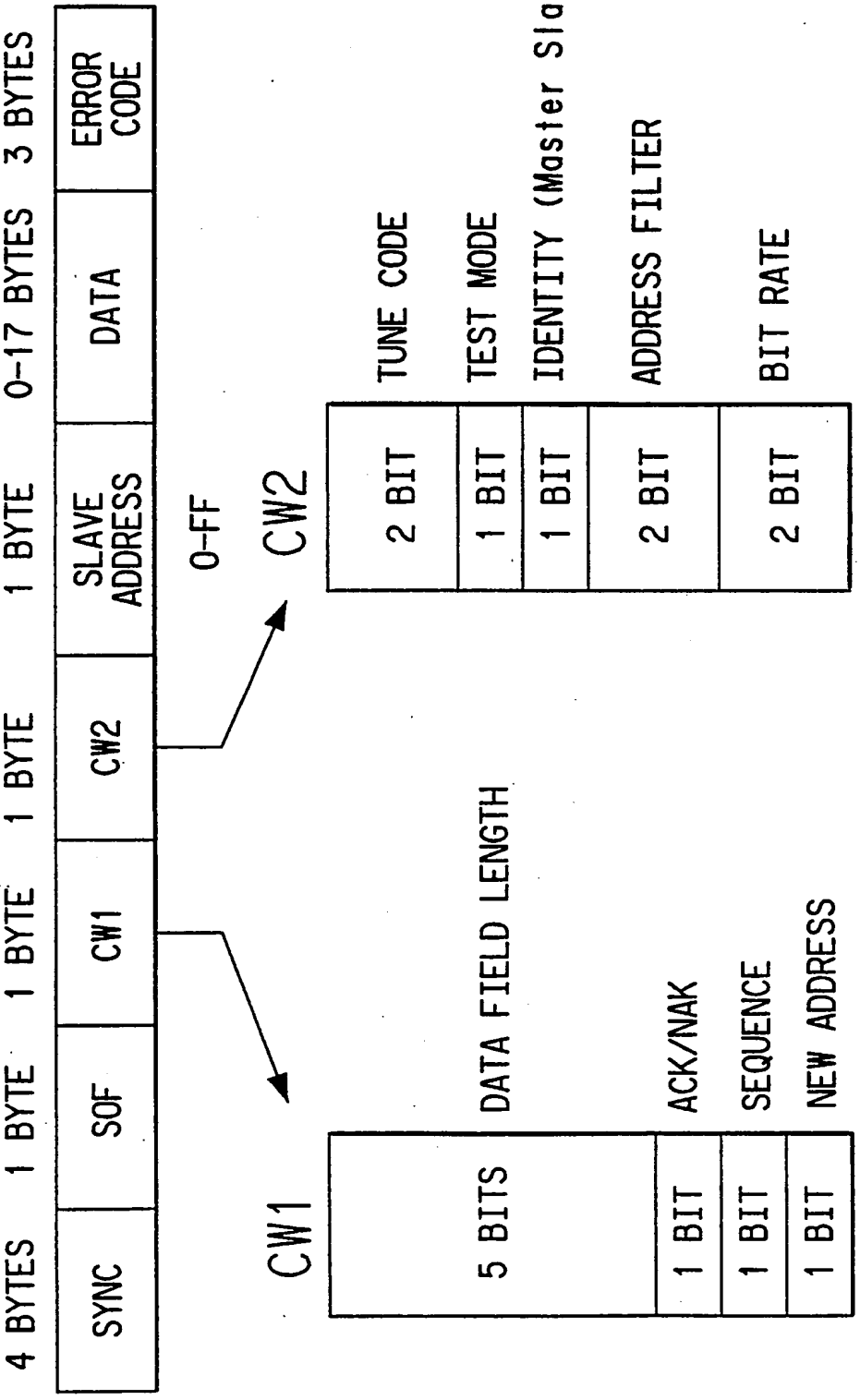

FROM FIG. 15
TO FIG. 15
PARITY OK ?
NO
YES
FETCH CORRESPONDING BYTE FROM MSG BUFFER
STORE BYTE TO MSG BUFFER
ADD BUFFERED BYTE (FROM PREVIOUS PACKET) TO EDC
ADD BYTE TO EDC
INCREMENT BYTE COUNT
BYTE COUNT > PACKET LENGTH ?
NO
YES; PACKET COMPLETE
EDC = 0 ?
YES; VALID PACKET
PROCESS & ACKNOWLEDGE PACKET
REQUEST RETRANSMISSION

FIG.16


4 BYTES
SYNC
1 BYTE
SOF
1 BYTE
CW1
1 BYTE
CW2
1 BYTE
SLAVE ADDRESS
0-17 BYTES
DATA
3 BYTES
ERROR CODE
0-FF
CW1
5 BITS
DATA FIELD LENGTH
1 BIT
ACK/NAK
1 BIT
SEQUENCE
1 BIT
NEW ADDRESS
CW2
2 BIT
TUNE CODE
1 BIT
TEST MODE
1 BIT
IDENTITY (Master Slave)
2 BIT
ADDRESS FILTER
2 BIT
BIT RATE

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/06911

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :Please See Extra Sheet.
US CL :371/5.1, 5.2; 375/8, 10, 98, 109.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 371/5.1, 5.2; 375/8, 10, 98, 109.

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS (bit error rate (P) gain control)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A, 4,291,410 (CAPLES ET AL) 22 September 1981, col. 2, lines 9-13, col. 7, lines 56-67 to col. 6, lines 1-3, col. 5, lines 27-28.	1, 6, 11, 14
Y	US, A, 5,093,842 (GIMLIN ET AL) 03 March 1992, col. 1, lines 14-25, col. 4, lines 24-29.	1, 11, 14
Y	US, A, 5,029,182 (CAI ET AL) 02 July 1991, col. 1, lines 45-55, col. 6, lines 21-26.	1, 11, 14
A	US, A, 4,387,461 (EVANS) 07 June 1983, Abstract.	1, 11, 14

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 08 OCTOBER 1993	Date of mailing of the international search report NOV 24 1993
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. NOT APPLICABLE	Authorized officer STEPHEN CHIN Telephone No. (703) 305-4700

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/06911

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A, 4,756,007 (QURESHI ET AL) 05 July 1988, col. 1, lines 40-55, col. 2, lines 5-65.	5, 11
A,Y	US, A, 5,048,054 (EYUBOGLU ET AL) 10 September 1991, col. 3, lines 5-15 and 45-68.	5, 6, 9, 11
Y	US, A, 4,823,344 (YONEHARA) 18 April 1989, col. 1, lines 33-44.	7, 8, 14
Y	US, A, 5,046,066 (MESSENGER) 03 September 1991, col. 3 and col. 4.	7, 8, 14

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/06911

A. CLASSIFICATION OF SUBJECT MATTER:
IPC (5):

H04J 13/00, 3/24; G06F 11/00; H04B 1/38, 3/46, 17/00; H04L 27/08, 7/00.